DN 99/323

REC'D 07 JUL 1999
WIPO PCT

THE UNITED STATES OF AMERICA

TO ALL TO WHOM THESE PRESENTS SHALL COME:

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

May 20, 1999

THIS IS TO CERTIFY THAT ANNEXED HERETO IS A TRUE COPY FROM THE RECORDS OF THE UNITED STATES PATENT AND TRADEMARK OFFICE OF THOSE PAPERS OF THE BELOW IDENTIFIED PATENT APPLICATION THAT MET THE REQUIREMENTS TO BE GRANTED A FILING DATE UNDER 35 USC 111.

APPLICATION NUMBER: ***60/088,978***
FILING DATE: ***June 11, 1998***

PRIORITY DOCUMENT

SUBMITTED OR TRANSMITTED IN COMPLIANCE WITH RULE 17.1(a) OR (b)

By Authority of the
COMMISSIONER OF PATENTS AND TRADEMARKS

T. Wallace
T. WALLACE
Certifying Officer

06/11/98 JC585 U.S. PTO

PROVISIONAL PATENT APPLICATION

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400
Facsimile: (703) 836-2787

ATTORNEY DOCKET NO.: 100878

DATE: June 11, 1998

BOX PATENT APPLICATION

PROVISIONAL PATENT APPLICATION
RULE §1.53(c)

Sir:

Transmitted herewith for filing under 37 CFR §1.53(c) is the provisional patent application of

FIRST INVENTOR: Niels Ole NIELSEN

RESIDENCE: Silkeborg, Denmark
(City and Either State or Foreign Country)

SECOND INVENTOR: Armin DELONG

RESIDENCE: Brnå , Czech Republic
(City and Either State or Foreign Country)

THIRD INVENTOR: Vladimir KOLARIK

RESIDENCE: Brnå , Czech Republic
(City and Either State or Foreign Country)

FOR (TITLE): PLANAR ELECTRON EMITTER (PEE)

09/106,238 06/11/98

- ☒ Formal drawings (Figs. 1-24; sheets 24) are attached.
- ☐ An assignment of the invention to _____ is filed herewith.
- ☐ A statement to establish small entity status under 37 C.F.R. §§1.9 and 1.27 is filed herewith.
- ☒ A check in the amount of $75.00 (Check No. 60036) to cover the filing fee is attached.
- ☒ The Commissioner is hereby authorized to charge payment of any additional filing fees required under 37 C.F.R. §1.16 or credit any overpayment to Deposit Account No. 15-0461. Two duplicate copies of this sheet are attached.

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

JAO:JAS/mdo

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Jay A. Stelacone
Registration No. P-42,168

1. Title of the Invention

Planar Electron Emitter (PEE)

2. Abstract

A planar electron emitter, based on the existence of quasi-ballistic transport of electrons is disclosed. In its preferred embodiment the planar electron emitter structure consists of a body of finite gap *pure* semiconductor or insulator, the said body of *macroscopic thickness (~1 mm)* being terminated by two parallel surfaces and of a set of two electrodes deposited on the said two free surfaces such that when *a low external electrical field (~100 V/cm)* is applied to this structure, consisting of two electrodes and the said semiconducting or insulating body sandwiched between them, a *large* fraction of electrons injected into the said semiconductor or insulator body from the negatively charged electrode (cathode) is quasi-ballistic in nature, that is this fraction of injected electrons is accelerated within the said semiconductor or insulator body without suffering any appreciable inelastic energy losses, thereby achieving sufficient energy and appropriate momentum at the positively charged electrode (anode) to be able to traverse through the said anode and to escape from the said structure into empty *empty space* (vacuum).

A number of apparatuses, using the said (disclosed) planar electron emitter in various fields of application, are also disclosed and the priority rights for the said apparatuses are also claimed.

3. Introduction

The present invention relates to a general class of electron devices termed "electron sources" and more specifically to a subclass termed "planar electron sources".

All of these devices provide a beam of electrons that can move through the vacuum and be used for various purposes (technological applications).

The essential requirement for all electron sources is to provide sufficient amount of electrons at the emittining surface of the device (the surface of the device facing the vacuum) with sufficient amount of energy (3-5 eV in most cases) and velocity (velocity component in the direction of emitting surface-empty space) in order that these electrons can surmount the energy barrier at the emitting surface - vacuum interface (this energy barrier being given by the energy difference between the vacuum level and the electron chemical potential at the emitting surface) and therefore can escape from the material into vacuum.

The neccessary amount of energy can be supplied either by heating the emitting surface ("Thermal emission" electron sources), by establishing a sufficiently high electrical field in the region emitting surface - vacuum ("Field emmision" electron sources), by sufficient acceleration of electrons within the bulk region of the device in the direction towards the emmiting surface ("Tunnelling field emmision" and/or "Quasi-ballistic field emmision" electron sources), by illumination of the emitting surface with help of photons or other energetic particles ("Photo emission" electron sources) or by lowering of the said energy barrrier at the emmiting surface-vacuum interface ("Negative electron affinity emmision" electron sources).

In some devices a combination of the above methods is used in order to achieve the most optimal performance as for example in "Thermal, field emmision electron sources" .

The applications of electron source devices typically include all forms of electron microscopy (and derivations there-off , such as electron beam lithography for example),

electron guns for evaporation of materials, x-ray tubes, electron multipliers (photomultipliers), electron beam welding machines and many other electron beam applications (standard TV screens).

While for some applications a point source electron beam is required, which is subsequently accelerated and electron optically modulated, there is a large number of technological applications, where a planar source of electrons is required and/or would be advantageous. Planar electron beam lithography, Flat Panel Displays (based on electron field emission), emission electron microscopy, two dimensional particle/elec.mag. radiation detector arrays and some fast ballistic semiconductor components and devices are just few examples of these applications.

The existing field emission planar electron sources (devices) suffer from a number of shortcomings, the most important being the instability, short life-time, too large electrical power consumption per square centimetre of electron emitting surface, the complexity of construction and too high cost.

The present invention aims at solving all of these shortcomings by using the discovery of the existence, under proper operating conditions and in certain simple semiconductor and insulator structures (devices), of the quasi-ballistic electrons in the said structures.

4. Description of drawings

In order to facilitate the analysis of the prior art and the description of the present invention, the following figures and/or drawings will be used:

Figure 1 is a schematic and simplified electron energy band diagram according to present invention, when the applied external potential is zero.

Figure 2 is schematic and simplified electron energy band diagram according to present invention, when a finite external potential is applied .

5. The state of the art (Background of the invention)

To the best knowledge of the authors , there is no prior art to the present invention - *Quasi-ballistic, field emmision electron source*. There is however a very large number of inventions, as can be seen for example from citations in the US patent n. 5.703.435 (December 1997) and the US patent n. 5.534.859 (September 1996), that all relate to planar electron emitter with the main emphasis on the use of these inventions as basic building blocks in field emission Flat Panel Displays.

All of these said prior art inventions (filed emission planar electron emitter devices) can be broadly devided into two classes.

In the first class electrons are emitted into the *empty* space between a cathode and the anode by applying sufficient electrical voltage between them. The emitting cathode in this case is usually either covered by a material with a low electron work function and/or it is geometrically shaped in order to facilitate electron field emission (US patent n. 5.703.435 and the citations there-off). In some cases the temperature of the emitting cathode is raised in order to increase the electron emission current Iem .

In the second class of the said prior art the emitting cathode - anode structures are usually *of all solid state construction and are* formed from a combination of metallic, semiconducting and insulating materials in order to establish the necessary conditions for the electron field emission to take place *at the anode surface-empty space interface* (U.S.patent n. 5.463.275, U.S.patent n. 4.303.930, U.S.patent

n. 4.801.994, British patent n. 1.303.659, European patent n. EP 0 504 603 B1, U.S.patent n. 5.554.859 and the citations there-off). For the electron - light conversion purposes , the appropriate "luminophors" materials can be incorporated within the anode structure, the said anode structure being either an integral part of the whole solid state cathode - anode structure or *part of it (the "accelalerating electrode" part)* being separated from the cathode-*anode structure* and the electron emitting surface by a finite empty space.

In some cases of the said prior art, the features characterising class one (formation/concentration and shaping of the necessary electrical field through geometrical shaping of the cathode structure and/or use of the low work function materials as a part of the electron emitting surface) and class two (combination of more or less planar metallic, semiconducting and insulating materials of various thicknesses) are combined (U.S.patent n. 5.444.328, U.S.patent n. 4.683.399, U.S.patent n. 5.212.426, U.S.patent n. 5.229.682, U.S.patent n. 5.528.103, European patent n. 0 150 885 B1, European patent n. 0 601.637 A1, U.S.patent n. 5.340.997 and the citations there-off).

The drawbacks of the said prior art devices are among others power consumption, limited life-time, use of non-standard expensive materials, insufficient stability, the necessity of generating high electrical fields over very short distances, the complexity of the necessary technological steps during their manufacture, low electron emission efficiency, scaling-up problems and cost.

It is a particularly characteristic feature of a majority of solid state devices in class two of the said prior art that the *neccessary , large external voltages have to be applied over relatively very short distances (of the order of the electron mean free path)* in order to generate sufficiently strong electric fields *(see equation (1) for the relation between the electrical potential V and the electrical field E)*

that facilitate the generation and the acceleration of electrons. *These electrons* then travel *along what could be called quasi-ballistic trajectories* in the said strong electric field (usually undergoing also an avalanche multiplication here) towards the surface of the (emitting) anode. *At the same time however, they loose, on their way,* an appreciable amount of energy through inelastic collisions (scattering) .

Therefore, either only a small portion of these electrons have sufficient energy to escape through the (emitting) surface of the anode into a space next to the cathode - anode structure *(situation at lower fields and larger distances travelled), or the life-time of these said devices in the prior art is short due to irreversible damage caused by dielectric breakdown effects and/or overheating due to large energy losses in the critical areas of the said devices (high electric fields over very short distances).*

Devices of this type include for example various forms of Metal-Insulator-Metal electron field emitters (Physical Review Letters Vol. 76, N.17 (1996), 320), p-i-n junction, p-n junction and Schottky barrier electron field emitters (U.S.patent n. 4.801.994, European patent n. EP 0 504 603 B1, U.S.patent n. 5.554.859, U.S.patent n. 4.303.930, British patent n. 1 303 659 and the citations there-off), various heterojunction electron field emitters (U.S.patent n. 5.463.275), but also electron field emitters containing various forms of diamond-like components (U.S.patent n. 5.631.196, U.S.patent n. 5.703.435, U.S.patent n. 5.536.193 and the citations there-off).

These devices have therefore in general quite low electron emission currents I-em (Fig. 2), high background current I-back (Fig. 2) , are often unstable and liable to dielectric breakdown that generally seriously limits their life-time. Also, scaling-up of these planar electron field

emission devices (increasing the electron emitting area of the cathode) poses a severe problem.

It is the aim of the present invention to provide a planar electron emitter that does not suffer from the above mentioned drawbacks.

The present invention addresses one of the fundamental problems encountered in the said prior art devices , namely the requirement of relatively very high local electrical fields over relatively very short distances. This requirement , *together with the quality of the material at hand,* lead in its consequence, to shorter electron mean free path (larger scattering rates) that in turn effectively sets the limit on possible physical distances within the said devices that electrons can move through without too appreciable energy losses.

As will be shown below, the present invention is based on a discovery of macroscopic quasi-ballistic trajectories (distances travelled *by quasi-ballistic electrons that are many hundreds of microns long)* that some electrons follow in a piece of *properly chosen and prepared* semiconductor or insulator material , when the said piece of semiconducting or insulating material is subjected to low applied external electric fields *(~100 V/cm)*.

6. Description of the present invention (Detailed and specific description of the invention)

6.1. Introduction

The present invention will be now disclosed (described) with reference to figures (Figure 1 and Figure 2). Also, for the sake of clarity, without loosing the validity and generality of the arguments to follow, a simplified model will be used that also uses a specific set of electrodes.

Under no circumstances this should be construed as limiting factor of the present invention. The specific configuration in Figure 1 and Figure 2 is used purely for illustration purposes and other much more general and/or different configurations are possible and must be considered as covered by the present invention.

In Figure 1, a simple electron band structure as a function of spatial co-ordinate of a piece of semiconductor or insulator material is shown, where two, *for the electrical transport most relevant,* quantum mechanical energies Ev (top of the valence band) and Ec (bottom of the conduction band) are marked. The two energies Ec and Ev are separated by a band gap Eg. A set of two metal electrodes ,metal electrode 1 *(cathode)* and metal electrode 2 *(anode),* are deposited on the two respective surfaces S2 and S3 of the said piece of semiconductor or insulator material. For the sake of simplicity these two electrodes are assumed to be identical.

At zero degrees Kelvin all quantum mechanical electron states above Ec and above chemical potential μ^{ch} of the metal electrodes are empty, while those bellow Ev and bellow chemical potential μ^{ch} of the metal electrodes are occupied.

At some finite temperature , let us say 300 degree Kelvin and in thermodynamical equilibrium, the chemical potential within the bulk of the said piece of semiconducting or insulating material μ^{ch} is assumed to lie somewhere near the midgap. For the sake of simplicity it is assumed that this chemical potential coincides (in energy) with the chemical potential of the metal electrodes, forming in this way what is known as a neutral electrical contact. At this finite temperature there will be a small but finite concentration "ne" of mobile electrons at energy Ec and small but finite concentration "nh" of mobile holes at Ev. It is assumed furthermore that the semi-classical approximation is valid which means that there are no changes in the electron band

structure locally when external electrical field E is applied. The effect of this field is accounted for by appropriate spatially dependent energy shift of all quantum mechanical energies at a given distance x due to the presence of the classical electrical potential

$$V(x) = E \cdot x \qquad (1)$$

Figure 1 then describes in its totality the situation at finite temperature when no external electrical field is applied.

The situation described in Figure 1 will change to situation described in Figure 2, when a finite, negative electrical charge ΔQ is added to metal electrode 1 and corresponding negative electrical charge ΔQ is removed from metal electrode 2. These extra charges on the two said electrodes will cause a constant electrical field E to be present within the said piece of semiconducting or insulating material.

Under low, ohmic electrical field E (~ 10^4 V/cm ; see also Figure 2) , the *mobilities* and the concentrations of thermal electrons and holes (Figure 2) will stay essentially constant, while their drift velocities will change accordingly

$$\text{v-drift (electrons;holes)} = \text{mobility (electrons;holes)} \cdot E, \quad (2)$$

increasing in this way the respective currents "Ie" and "Ih" (Figure 2) with increasing applied electrical filed E . The component "Ibal" (Figure 2) is the contribution to the total electrical current running through the structure shown in Figure 2 from *quasi*-ballistic electrons, that is those electrons, injected into said piece of semiconducting or insulating material from the metal electrode 1, that essentially do not suffer any inelastic energy losses nor any appreciable momentum changes while moving through the said

piece of semiconducting or insulating material towards the metal electrode 2 along the electron quasi-ballistic trajectory shown in Figure 2. *The electrical current component "Iem" is due to those electrons (quasi-ballistic electrons) which, after traversing from the metal electrode 1, through the said piece of semiconducting or insulating material and into the metal electrode 2, have still sufficient energy (energy larger than the energy barrier of the emmiting surface S4 - Free Space interface) and finite, sufficiently large velocity component in x- direction in order to escape from the structure ,composed of the metal electrode 1 plus the said piece of semiconducting or insulating material plus metal electrode 2, into free space "FS" (Figure 2) through electron emitting surface S4 (Figure 2).*

6.2. The essential aspects of the present invention

In what follows, a detailed and specific description of the preferred embodiment of the present invention - Quasi-Ballistic Planar Electron Emitter short - Planar Electron Emitter (PEE)) will be given through description of the essential aspects and characteristic features of the present invention., The emphasis will be on the Discovery aspect, Technical Novelty aspect and on the comparison with the present day understanding of the phenomenon in question. The crucial role, played by the former patent by one of the authors of the present invention in the said, unexpected discovery will be also stressed.

6.2.1. The present understanding of ballistic transport phenomenon

The present understanding of the essential physics of this (quasi)-ballistic transport process (Karl W. Boer : "Survey of Semiconductor Physics", Volume II, Van Nostrand

(NY), 1992, S.M.Sze : "Physics of Semiconductor Devices", John Wiley & Sons (NY), 1981) is that, as long as the applied electrical field E (Figure 2) is within ohmic range (mobile charge carriers' concentrations and electrical mobilities constant and electric field E independent) and the thickness of the said piece of semiconducting or insulating material "Lsam" (Figure 2) is larger than the mean free path of the mobile charge carriers (at best of the order of some one to two thousand Angstroms), the electrical current component "Ibal" is negligibly small, leading to essentially zero value of the electron emission current "Iem" (Figure 2).

6.2.2. Discovery aspect of the present invention

The discovery that this present day understanding of the essential physics of ballistic transport in relation to pure semiconductors and insulators is not correct forms the basis of the present invention.

This discovery was made possible through the use of the Electrical Impedance Spectroscopy (EIS) experimental method according to the patent by one of the authors of the present invention
(US Patent n.: 5 627 479 (May 1997), European Patent n.: EP 0 672 257 B1 (February 1998) , both entitled "Method and apparatus for determining characteristic electrical material parameters of semiconducting materials"). The EIS measurement and analysis of the electrical response in pure, single crystal silicon has predicted a relatively very large electron emmision current "Iem" (see Figure 2) .

This prediction was then confirmed by an experimental observation of a large, finite electron emmision current "Iem" (of the order of "Ibal" + "Ie" ; see Figure 2), when a 0.5 millimeter thick, contacted, single crystal silicon sample has

been biased by no more than some 3.5 - 4.0 Volts, in an experimental configuration as shown in Figure 3.

In reference to Figure 3 now, the quasi-ballistic semiconductor (QB-Sem) in this case was the said single crystal silicon sample, cut out from a single crystal Si ingot, prepared by a Float Zone crystal growth method. Thin slices (wafers) were prepared from this ingot, with <111> orientation perpendicular to the wafer surface. Both surfaces S2 and S3 were optically polished. The Phosphor doping level (giving n-type conductivity) was chosen to be $2.0 \cdot 10^{12}$ cm^{-3} *. A Schottky contact (a cathode) was prepared by a successive evaporation of 50 Å of Cromium onto the surface S2, followed by evaporation of 2000 Å of Gold. The anode was ohmic, consisting of high Phosphor concentration, degenerate silicon layer (a thin region of some 1~5 microns thick, below the surface S3 - see Figure 3) and a thin 150 Å thick evaporated Gold film. The sample was placed in the vacuum and at external voltage of some 4.0 Volts (forward bias) between the cathode and the anode (at four volts across 0.5 millimeter - the thickness of silicon sample, the electric filed of 80.0 Volts/cm was created within the bulk of the silicon sample) a finite, relatively large and laterally homogeneous electron emmision current "Iem" was observed. The magnitude of the emmision current "Iem" indicated that as much as some 30 % of all electrons , injected into the silicon sample from the cathode, reached the anode with energies of some 4 electron volts (electron affinity in silicon is 4.0 electron volt) above the energy "Ec" (see Figure 2), sufficient in order for these electrons to surmount the energy barrier of the anode surface S4 - vacuum interface and to escappe into the free space FS (see Figure 3).*

This result constitutes the following <u>essential discovery aspect of the present invention</u>:

"Contrary to the present day understanding of the neccessary conditions for the occurrence of ballistic transport in various materials, a relatively large portion of electrons injected into pure silicon follow quasi-ballistic trajectories already at low levels of the applied electric field (below 100 V/cm). These trajectories are spatially macroscopic (of the order of millimeters) and the said electrons (quasi-ballistic electrons) , moving along these trajectories from one end of the silicon sample (surface S2) to the other end (surface S4) are accelerated, increasing thereby their energy, and escape into vacuum through the electron emmiting surface S4" .

6.2.3. Technical Novelty aspect of the present invention

The quasi-ballistic electrons that move within the said piece of silicon sample (from now on also referred to as Quasi-ballistic semiconductor - "QB-Sem", stressing the fact that silicon is not the only possible material) suffer almost no energy losses and momentum changes during their movement from the cathode to the anode. This means that no heat is generated within the said silicon sample. Firthemore, the relation between "Iem" , "Ibal" and "Iback" (Figure 2), together with simplicity, robustness of the said structure (Figure 3) and the fact that the quasi-ballistic transport in the said piece of Quasi-ballistic semiconductor (silicon sample as described above) is possible at low (ohmic) electrical fields and can take place over macroscopic distances makes the said structure an almost perfect planar electron emitter with substantial technological implications. The said planar electron emitter depicted in Figure 3 and comprising the said structure constitutes then the Novelty aspect of the present invention.

The number of technological applications of the present invention - the said planar electron emitter, is very large and it is the intention of the authors of the present invention to claim also the use of the present invention in these. These applications include methods and apparatuses/products such as Planar electron beam lithography, Field emission Flat Panel Displays, High speed (low-dissipation) signal transmission devices, High efficiency detectors, efficient Light sources, Electron emission microscopy, Two-dimensional electro-magnetic radiation and/or particledetector arrays, High speed, easily integrable semiconductor components, Semiconducting devices using ballistic electrons, variety of (novel) electron sources and many others.

7. Examples of Applications (Description of the preferred embodiments)

A number of applications of the present invention will be now illustrated and discussed in some detail with reference to Figures 3 to 24 . The generality of each application field using the present invention has to be stressed at this time , although each application field and/or product will be illustrated with a help of a specific preferred embodiment and relevant figure(s). To each such preferred embodiment there exists a large number of other embodiments and/or modifications of the preferred embodiment, that all use the present invention as a crucial component. Therefore it is essential that the description of the present invention already given in chapter 6 and the description of the applications of the present invention to be given in the following, are not construed as limiting the scope of the present invention and its applications.

In the following text and the accompanying figures the following convention will be used:
"a piece of semiconducting or insulating material" is referred to as quasi-ballistic semiconductor (QB-Sem)

7.1. Planar Electron Emitter (PEE) (A detailed specific summary of the present invention)

Figure 3 is a schematic diagram illustrating one of possible physical forms of the present invention - the preferred embodiment of the Planar Electron Emitter (PEE) according to present invention.

The region 1 (a cathode) is connected both to region 2 (a piece of quasi-ballistic (QB) semiconductor) via surface S2 and to a negative pole of an external electrical charge/voltage supply 8 (battery) via electrical contact pads ECP . Its role (cathode) , together with the battery, is to supply and to maintain the negative electrical charge ΔQ (electrons) on the surface S2. At the same time , the same negative electrical charge ΔQ is removed from the region 4 (anode). The anode is connected to region 2 via surface S3 and to a positive pole of the external charge/voltage power supply 8 via ECP, the said power supply 8 maintaining the surface S3 positively charged. In this way a uniform electrical field E is established between the surfaces S2 and S3 , causing a finite electrical current "Itot" to flow through the region 2. In reference to Figure 2 now, this electrical current "Itot" is composed of three components "Ie" , "Ih" and "Iem". While the first two components form the background electrical current "Iback", the component "Iem" is formed by that portion of the electrons (from now on termed as quasi-ballistic (QB) electrons) that physically leave the device and enter the free space FS (Figure 3) if a sufficiently high electrical field E and the corresponding electrical potential

difference $\Delta V = E \cdot t1$ is maintained between the surfaces S2 and S3 .

When a piece of semiconducting or insulating material (region 2 - from now on termed as quasi-ballistic semiconductor (QB-Sem)) is properly prepared *(see chapter 6 for specific description)*, the surfaces S2 and S3 are properly treated and the regions 1 and 2 are properly chosen and constructed , the part of the electrical current "Iem" (electron emission current) can become quite large in relation to the background current "Iback".

When QB semiconductor is properly *chosen and prepared (see chapter 6)*, then even without any efforts for optimisation (inclusive the optimisation of the surfaces S2 and S3) , "Iem" of hundreds of nano-Amperes per square centimetre can be measured at electrical fields of the order of some 100 Volts/cm (from now on termed as ohmic electric fields), with the total thickness of the device L2 being macroscopic (millimetres). With the length scale L1 (square root of the area of the device) being of the order of 30 cm (today's size of silicon wafers for example), the device depicted in Figure 3 is a large area planar electron emitter that is very simple to manufacture and can be produced at a very competitive price. In one of the obvious applications, namely the flat TV screens, this price is competitive even when compared with the standard Cathode Ray Tube (CRT) TV screens.

The Planar Electron Emitter (PEE) according to the present invention has been now demonstrated through a description of one preferred embodiment shown in Figure 3. There exists however a large number of other embodiments, all according to the present invention, that relate to different choise of materials, of design and of preparation and construction of the said Planar Electron Emitter, the said differences being dictated by the requirements of the applications at hand.

Therefore, few specific comments will be now made and some examples will be given regarding the preferred and other embodiments of the present invention (PEE), adressing all the essential parts of the PEE as depicted in Figure 3. All this in order to make the description of the said Planar Electron Emitter according to the present invention and the use of the said PEE in various technological applications as complete as possible:

The region 2 - Quasi-ballistic semiconductor

The choise of the quasi-ballistic semiconductor is not limited to one particular material, but can be prepared in a number of different ways, using different materials . The only requirements are the existence of a finite band gap Eg (see Figure 1) and the existence of quasi-ballistic trajectories for electrons between the two opposite surfaces of the material. In the preferred embodiment the said material (QB-Sem) is silicon, but group III - V compound semiconductors (such as GaAs) and group II - VI compound semiconductors are also equally good candidates. Crystallographic orientation, shallow and deep impurities doping levels and the temperature of operation of the finished device are the important parameters to consider when choosing a suitable quasi-ballistic semiconductor.

Also well suited as Quasi-ballistic semiiconductor(at least in principle) are insulators such as SiO2, Al2O3 , silicon nitride , diamond (or diamond-like Carbon particles) and others. Some of the materials have been and/or are being investigated in connection with their use as field emission electron sources already (see chapter 5: State of the Art).

2. Region 1 and surfaces S1 and S2 - Cathode region

In the preferred embodiment described in Chapter 6 and depicted in Figure 3, the cathode region has been formed by evaporation of Chromium and Gold metal films onto the surface S2 of the silicon sample, forming in this way a rectifying Schottky contact.

The sole purpose of the cathode region though is to mantain various amount of negative charge ΔQ on the surface S2 and this can be done in a number of different ways.

In one such alternative, the region 1 is just a gaseous phase of partially ionised gas such as Argon and/or Nitrogen. No metal electrode is required in this case at all.

To achieve the optimal performance of the cathode as an electron injector of electrons into QB-semiconductor (region 2), it is desired that the said extra negative charge ΔQ from the battery (see Figure 3) moves the chemical potential μ^{Eh} (see Figure 2) as much as possible (increase of the electron injection into QB-Sem). This can be achieved by decreasing the interface electron density of states through mechanical, chemical and/or thermal treatment of the surface S2. If the metal cathode electrode is either required or desired, this treatment of the surface S2 is done prior metal material deposition. Alternatively, one can choose a metallic material with low electron density of states at the Fermi level and/or low electron work function .

Region 4 and surfaces S3 and S4 - Anode region

In the preferred embodiment described in Chapter 6, a thin region of silicon sample, next to the surface S3, has been implanted with high dosis of Phosphorus, becoming in this way degenerate. A thin Gold film has been then deposited on the said surface S3 which has been optically polished prior this Gold film deposition, the whole structure forming in this way

an ohmic contact to the silicon sample. This preparation of the anode region might not lead to the most optimal performance of the said Planar Electron Emitter PEE.

As with the cathode region, the sole purpose of the anode region is to secure that a various amount of the negative charge ΔQ can be removed from the surface S3 region . Here though, the requirements concerning the optimal functioning of the said (anode)region are different from those valid for the cathode region . The hole current "Ih" (see Figure 2) should be minimised (current "Ih" increases as the interface chemical potential μ^{ch} moves downwards in energy - see Figure 2) as well as the thickness of the anode metal electrode (relatively large energy losses of the quasi-ballistic electrons when moving through region 4). To achieve the first of these goals one needs either a metal with very high electron density of states at the Fermi level and/or very high electron density of states within the surface 3 - region 4 interface. As with the preparation of the surface S2 , also here this can be achieved with the proper mechanical, chemical and/or thermal treatment of the said surface S3 prior metal deposition.

In order to achieve the second goal, yet another alternative can be chosen. In this case the surface S3 is free of the metal electrode (region 4 in Figure 3) and an extra electrode (accelerating electrode 7 - see Figure 8 for example) is placed within the free space FS (Figure 3) and in closed vicinity of the surface S3 . This extra electrode is biased at relatively high positive potential with the respect to surface S3 and/or the cathode region 1, polarising in this way the whole assembly. If the developed electric field within the region 2 is not sufficient for the acceleration of the quasi-ballistic electrons within the region 2 to energies required in order for these electrons to escape through the said surface S3 into free space FS, the surface S3 can be geometrically shaped

in such a way as to increase the said electric field locally at points (and/or sharply curved regions) of the surface S3, spatially closest to the to the accelerating electrode 7.

Finally, the geometrically shaped surface S3 can be covered by a thin metal electrode (serving as a anode), the whole Planar Electron Emitter assembly (inclusive the accelerating electrode 7) looking similar to an arrangement shown in Figure 8. In such an arrangement the electrical discharging/charging up effects on the geometrically shaped surface S3 are minimised.

The important point to stress here is that the shape of the electron emitting surface S3 (surface S4 if metal electrode 4 is present) does not have to be strictly planar.

Injection of electrons into Quasi-ballistic semiconductor

In the preferred embodiment described in Chapter 6 and depicted in Figure 3, a sufficient injection of electrons from the cathode into the silicon sample ("Injection of electr.charge" - see Figure 2) has been achieved electrically, by supplying the metal electrode 1 (cathode) with extra amount of negative charge ΔQ from the battery.

Other methods for electron injection have been described in the general discussion of electron sources in Chapter 3 and in the Section 7.1. of Chapter 7.

Since the electron injection from the cathode region into QB-semiconductor is also strongly temperature dependent, an alternative embodiment of the Planar Electron Emitter according to the present invention can involve a heated cathode structure (region 1 - see Figure 3).

In yet another alternative embodiment, the electrons are injected into QB-semiconductor by photo-illumination of the cathode - injecting surface S2 region (in some cases this region can include part of the QB-semiconductor next to the

surface S2) through the surface S1. This embodiment of the said Planar Electron Emitter PEE according to the present invention is particularly usefull in opto-electronic applications.

The technological use of the present invention covers not only the field of electron-optical applications , but also the design and production of semiconductor components and devices will benefit from the present invention. This is especially so because the quasi-ballistic electrons suffer no energy/momentum losses/changes while moving through the QB semiconductor. Their velocities are not limited by high electrical field mobility saturation effects and their behaviour is similar to the behaviour of electrons in vacuum tubes, only now no vacuum is necessary , the dimensions are small and the construction is all solid state. The existence, in QB-semiconductor, of ballistic electron trajectories over macroscopic distances and at low electrical fields have some obvious consequences :

1. The necessary geometrical scaling-down of various semiconductor components in order to obtain their faster response (high frequencies) is not necessary and new design/optimisation of these components and Integrated Circuits (ICs) can be undertaken.

2. The anomalously low power dissipation by QB-electrons within the QB-semiconductor contributes to the solution of the heat generation problem when high packing densities of components in the ICs are used.

3. Since the ballistic electrons in QB-semiconductor survive over macroscopic distances, the design of "Hot Electron" devices does not have to rely on thin film complicated multistructures that are often unreliable and costly to produce.

4. Because the quasi-ballistic electrons in QB-semiconductor do not require high electrical fields, the degradation of the various semiconductor devices through irreversible dielectric break-down is essentially eliminated.

In conclusion, the present invention can be summarised in the following few points:

1. In a properly prepared quasi-ballistic semiconductor, a portion of electrons (it is large enough to be technologically attractive) move along quasi-ballistic trajectories and can be accelerated by externally applied electrical fields to energies that are sufficient for their escape into vacuum.

2. The necessary externally applied electrical fields are low (< 100 V/cm).

3. The distances over which this "soft" acceleration of quasi-ballistic electrons takes place can be macroscopic (~millimetres).

4. The electron emission area is large and it is limited only by the lateral size of the QB-semiconductor wafer which is today some 800 cm2 (this limit can be of course overcomed by building modules).

5. The design and the structure of the Planar Electron Emitter according to the present invention is very simple.

6. The Planar Electron Emitter according to the present invention is characterised by a very low power dissipation.

The following important technological aspects of the present invention should be stressed :

1. Low power dissipation.
2. Simplification of the design/construction of various devices in th prior art.
3. Full integrability with the existing Semiconductor Technology

4. Full integrability with the existing Integrated Circuits' Technology/Production.
5. No geometrical constraints on the design of fast semiconductor components and devices.
6. No requirements of high electrical fields and/or very small dimensions when designing fast semiconductor components/devices.
7. No limit to geometrical scaling-up of electron emitting surface.
8. New design concepts for semiconductor components/devices and/or physical apparatuses are possible.
9. Robustness.
10. Life time of the same order of magnitude (or longer than) as the usual Semiconductor Industry products.
11. Low cost due to the simplicity of design.

7.2. Field Emission Flat Panel Displays (FE-FPD)

One of the obvious applications of the present invention is its use in the construction of robust, reliable, large, low power dissipation and cheap Field Emission Flat Panel Displays (FE-FPD).

Figure 4 , which is a cross-sectional diagram along the line A - A of the FE-FPD shown in Figure 5 is one of the possible vacuum-less FE-FPDs according to the present invention. With reference to Figure 3 , the basic planar structure of the present invention - 1(cathode), 2(QB-Sem) and 4(anode - optically transparent in this preferred embodiment) is clearly apparent also in Figure 4. The only difference is that in this Flat Panel Display application of the present invention the cathode and the anode are patterned and that an extra layer 3 (also patterned) is introduced between the surface S3 of the QB-semiconductor and the anode 4. This third layer consists of alternative segments of red, yellow and

blue phosphors or other colour light emitting luminophors. The segments are separated from each other by light non-emitting , electron absorbing material.

The patterning of layers 1, 3, and 4 enables selective addressing ("switching-on" by application of the appropriate voltages) of the individual colour segments ("pixels") and is shown in Figure 5. Here the cathode 1 (in form of metallic parallel strips) is deposited onto the back surface S2 of the QB-semiconductor 2 . Red (R), Yellow (Y) and Blue (B) luminophor strips are deposited on the front surface S3 of the QB-semiconductor 2, in alignment with the said cathode strips, as shown in Figure 5. Finally the anode 4, also in form of metallic, parallel strips , is deposited on the top of the layer 3 , with anode metallic strips at right angles to the cathode metallic strips, as indicated in Figure 5.

The electrical leads 9 and 10 are attached to the respective metallic strips of the anode and the cathode via electrical contact pads ECP, the whole cathode - anode structure forming in this way selectively addressable matrix of single colour light emitting elements. The element (i , j) is switched on by applying an appropriate voltage between the line i - (cathode) and the line j - (anode). The electrical leads 9 and 10 are connected to the usual TV a.c circuitry that drives the whole FE-FPD shown schematically in Figures 3 , 4 , 5 , 6 and 7. The dimensions d1, d2, d3 and d4 of the pixel matrix can be optimised at will, using the standard semiconducting patterning technology to fit the spatial resolution requirements of FE-FPD at hand .

The typical over-all size L1 L2 of a "single chip" FE-FPD depicted in Figures 4 , 5 , 6 and 7 is at present of the order of 20 cm · 20 cm, with the availability of 30.0 cm diameter Si wafers. When large colour displays are needed, a arbitrary number of "single chip" modules can be joined together on an appropriate substrate, using the segments d2 and d4 (see Figure 5) as joining regions, preventing in this

way the spatial degradation of the formed optical image quality.

The thickness L3 of the said FE-FPD depicted in Figures 4 , 5 , 6 and 7 is of the order of one millimetre, this thickness being essentially the thickness of the QB-semiconductor wafer.

In Figure 6, the layers 3 and 4 are switched over in order to illustrate yet another possible physical form of the said FE-FPD. Here the colour light layer 3 faces directly the free space FS. If needed, the surface S5 can contain a protective, transparent (anti-reflection) coating.

It has to be stressed at this point that the segments 5, 6 and 7 shown in Figures 4, 5, 6 and 7 do not have to be necessarily luminophors. The colour light emitting layer 3 represents also other types of ballistic electrons to colour light conversion materials and/or devices . One such type is an arrangement which can be described with the help of Figure 4 . In this case the structure 1(cathode) , 2(QB-semiconductor) , Red (Yellow, Blue) elements 5, 6 and 7 and 4(anode) form a matrix of Colour Light Emitting Diodes (CLED). Other FE-FPD arrangements , using the present invention are of course also possible and the preferred embodiment shown in Figures 5 , 6 and 7 should in no way considered as a limiting the scope of the present invention in this field of application.

Finally, in cases where the requirement of colour definition, brightness and colour contrast are not met with luminophors and/or other electron - light conversion elements/devices that are at hand today, the standard TV colour phosphors may be still needed that require quite high electron energies (high acceleration voltages in the region of some 10 to 20 kV). A vacuum Field-Emission Flat Panel Display may be then still a most optimal solution and one possible physical form, using the present invention, is shown in Figure 7.

In this configuration, the colour light emitting layer 3 shown in Figures 4, 5 and 6 is removed from the basic planar electron emitter structure 1(cathode), 2(QB-semiconductor) and

4(anode) and it is deposited on the optically transparent (glass for example) plate that forms, together with parts 14 and 12, the vacuum encapsulation of the said vacuum FE-FPD. The acceleration electrode 1 that is deposited onto the layer 3 is biased to the appropriate high positive voltage. This arrangement secures that the quasi-ballistic electrons that leave the basic planar electron emitter structure (attached mechanically to the base plate 12 via mechanical supports 15) through the surface S4, are accelerated within the free space FS (now vacuum) to sufficiently high energies in order to secure the proper functioning of the standard colour TV phosphors 5, 6 and 7.

The thickness (Dim 2) of the vacuum FE-FPD shown in Figure 7 is of the order of one to two centimetres, while the area (Dim 1) is unchanged in relation to the previously described vacuum-less FE-FPD.

<u>7.3. Planar Electron Beam Lithography</u> (1 : 1 electron stepper as an example)'

A second very important application of the present invention is in the field of Lithography (Microlithography) and more specifically in the field of what has been termed in the literature as Planar Electron Beam Lithography (PEBL). Lithographic steps are essential during the process of Integrated Circuit (IC) production. The lithographic part of IC production consists in principle in repetition of the steps of resist deposition onto the surface of the wafer, of the exposure to radiation of parts of the resist (through a mask and an appropriate projection system and/or by "direct writing" tool) and finally of resist removal. Optical, x-ray and Electron/Ion Beam Lithographies are the known methods that can, at least in principle, accomplish the necessary lithographic tasks during the IC production, the optical

lithography being the standard, well matured industrial technology. Its major drawback is the "optical" limit on the smallest features that can be "printed". For high frequency components/devices and in the further strife for decreasing the size of the IC components and ICs in general, this has to be considered as a major drawback .

Two of the authors of the present invention have shown and demonstrated experimentally (see Figures 11, 12, 13 and 14) how to solve this problem in principle, using Planar Electron Beam Lithography concept (H. Ahmed et al. eds : "Proceedings of the Conference on Microlithography" ; Cavendish Laboratory, Cambridge 1989). In this prior art, the electron lithographic projection system has been demonstrated. It consists of a planar source of electrons that emerge only through certain parts of the electron emitting surface. These electrons are then projected onto the wafer with pre-deposited electron sensitive resist layer.

The schematic diagram of the principle behind the Planar Electron Beam Lithography, used in this prior art, is shown in Figure 8. The whole structure shown in Figure 8 is placed in this preferred embodiment in vacuum.

A film of a metallic material (typically Aluminium) forming a cathode 1 is deposited onto a flat substrate 5 (typically glass or sapphire). The aluminium metallic film is then anodically oxidised forming an insulating thin film layer 2 (aluminium oxide). On top of this layer a required pattern 3 is formed by a standard sequential Electron Beam Lithography and finally a thin metallic anode 4 (typically 100 to 150 Angstrom of Au) is deposited on the said layer 3. The role of the said patterned layer 3 is to stop the electrons emerging through the thin insulating layer 2 from penetrating the anode and entering the free space FS .

The cathode 1 (metal), the thin insulating layer 2 (insulator) and the anode 4 (metal) form what is known in the prior art as Metal - Insulator - Metal (MIM) quantum

tunnelling structure. At sufficiently high voltage bias (supplied by the voltage source 8) between the cathode and the anode, a portion of electrons will quantum tunnel (Fowler - Nordheim tunnelling) from the cathode into the anode through the thin insulating layer 2. If however, a given portion of the anode is separated from the said insulating layer 2 by layer 3, the electrons will be absorbed in the said patterned layer 3. In other words, it will be only those parts of the whole MIM structure, where the anode 4 is in the direct contact with the insulating layer 2, that will allow the tunnelling electrons to enter the free space FS, provided that the applied external voltage between the cathode and the anode is sufficiently high, so that the tunnelling electrons gain sufficient amount of energy in order to surmount the work function barrier of the anode metal. Once in the free space FS, these electrons will be accelerated towards positively biased wafer 7 on the top of which a electron sensitive resist 6 has been deposited. Through the electron-optical means (1 : 1 projection, using parallel electrical and magnetic fields), the electrons that emerge for example at point i from the MIM structure shown in Figure 8 are imaged into point j, lying within the resist layer 6 . In this way the entire lithographic pattern (layer 3) can be transferred onto the said wafer - resist assembly at once and not sequentially as is the case with the standard Electron Beam Lithographers. Also, there are no principal limits on the lateral dimensions of the patterned layer 3 and this means that the entire wafer can be processed in one exposure. Furthermore, the minimum size features (the dimension "Min" in Figure 8) that can be easily obtained, using this prior art (~ 0.15 microns), are well bellow the present day limit of the standard optical lithography (0.2 - 0.5 microns).

One of possible alternatives to the embodiment shown in Figure 8 is shown in Figure 9. Referring to Figure 9 now, the same MIM basic structure of the planar electron emitter, as

discussed in reference to Figure 8, is clearly apparent. In the particular preferred embodiment shown in Figure 9, an accelerating electrode 11 and electron scintillator 9 structure has been inserted between the planar electron emitter MIM structure 1 , 2 , 3 , 4 , 5 and wafer 7 plus photo-resist 6 part. Such an arrangement allows for the planar electron projection system to be under vacuum (it is the region 9, 12 and 14 that form the vacuum encapsulation of the said MIM structure), operating continuously if necessary, while the wafers to be processed can be placed on the top of the scintillator 9, without a need for prior evacuation, thereby increasing the throughput of the whole device. If the air space, indicated in Figure 9 is sufficiently small, the degradation of the size of the minimum feature "Min" due to optical spreading can be kept to minimum.

In the said publication by two of the authors of the present invention, an apparatus - "Experimental 1 : 1 Electron Projection Stepper" has been disclosed and its performance that met all the industrial needs and requirements concerning the necessary lithographic steps during IC production has been clearly demonstrated. Its schematic diagram is shown in Figure 11. Here 1 is the said MIM cathode - anode assembly (very similar in construction to the arrangement shown in Figure 8 - parts 1, 2, 3, 4 and 5), 3 is the wafer substrate with the deposited resist layer 2, 4 is the x , y positioning table and finally 5 is a pair of Helmholtz coils to generate a homogeneous magnetic field between the cathode - anode assembly and the wafer - x,y table assembly. In this particular arrangement, it was the cathode - anode assembly that was negatively biased with the respect to the wafer substrate that was kept near ground potential. The emitted electrons have been accelerated in the established electrical field from high negative potential towards ground. The parallel electrical and magnetic fields formed in this way an electron - optical 1 : 1 projection system that transferred

the electrons emerging from a particular point on the bottom surface of the MIM cathode - anode assembly 1 to a single point within the resist layer 2 (see also Figure 8).

The over-all view of the said experimental 1 : 1 electron projection stepper is shown in Figure 12 and some typical experimental results of wafer patterning in Figures 13 and 14 . Both positive and negative resists were tested and with a typical exposure times of the order of 0.1 seconds, the minimum features easily attainable (length "Min" in Figure 8) were in the region of 0.15 microns (Figures 13 and 14). While a part of the whole ,exposed and patterned (repetition of test patterns) silicon substrate is shown in Figure 13, the structural details of the test patterns are shown in Figure 14, clearly demonstrating the 0.15 micron minimum feature capability of this prototype instrument.

Despite the fact that the experimental 1 : 1 electron projection stepper shown in Figures 11, 12, 13, and 14 satisfies all the most critical technological industrial requirements as a planar electron beam lithographic facility , it suffers from one major drawback which is the relatively very short life-time (only some 30 minutes of continuous operation in case of Al - Al2O3 - Au MIM planar electron emitter system).

By using the planar electron emitter according to the present invention, this major drawback of the said instrument is solved, offering a qualitatively new and robust solution to the present day needs of the semiconductor industry. One possible arrangement (a preferred embodiment according to the present invention) of such a planar electron emitter structure is shown in Figure 10. The only difference with the respect to the arrangement shown in Figure 8 and Figure 9, is the replacement of the thin film oxide layer 2 by the quasi-ballistic semiconductor QB-Sem. Turning now to Figure 10 , the electrons, emitted from the cathode 1 into QB-semiconductor 2 through the surface S2, travel along the

quasi-ballistic trajectories within the QB-semiconductor. They emerge, through the surface S3 and enter either the patterned absorbing layer 3 or the anode 4. The part of the quasi-ballistic electrons, not stopped by the electron absorbing layer 3, then have enough energy to enter the free space FS through the surface S4 as for example the electron at point i. These electrons are then accelerated within the free space region FS by biasing for example the wafer 7 and the resist 6 to sufficiently high voltage relative to the anode 4. Through the previously described electron-optical means (see Figure 11), the electron from point i (Figure 10) is transferred (imaged) to point j within the resist layer 6, securing in this way one to one (1 : 1) projection of the pattern 3 onto the resist 6. The minimum feature obtainable ("MinS") lies well bellow 0.15 micron, if the electron-optical system, together with the planar electron emitter part of the electron 1 : 1 projection stepper are optimised. Furthermore, by exposing the whole wafer at once, the throughput of such a planar electron beam lithographic system is very large. Although the Figure 10 shows an arrangement similar to Figure 8 , a number of other arrangements of planar electron lithographer are possible, an arrangement shown in Figure 9 being just one of them.

7.4. Two-Dimensional illumination panels

Due to the simplicity of design, robustness, low power dissipation, low temperature operation and two-dimensional nature of the planar electron emitter according to the present invention, the said planar electron emitter can be used very conveniently in the construction of two-dimensional (planar and non-planar) illumination sources.

One such possible flat illumination panel is shown schematically in Figure 15 and 16. Here the basic structure

of the planar electron emitter (cathode 1, QB-semiconductor 2 and the anode 4) is used as planar source of electrons (when an appropriate electrical voltage is applied between the cathode and the anode) emerging into the free space FS. These electrons are accelerated within this space by means of the accelerating electrode 11 and enter the light emitting layer 3. The optically transparent plate 13 (typically a glass plate) that allows the generated light to escape from the said structure forms (together with plates 14 and 12) the vacuum encapsulation of the whole assembly.

In another possible arrangement, the light emitting layer 3 is left out and the free space FS is filled with an appropriate gas and/or gas mixture, the necessary illumination being now generated through gas ionisation and fluorescence. The typical dimensions of the above described flat illumination are indicated in Figure 16. While "Dim1" - the thickness of the illumination panel can be easily under one centimetre, the "Dim2" can be easily of the order of meters.

Because of the simplicity of construction, the present invention can be used also in the construction of non-planar (round) two-dimensional illumination sources. One of the possible arrangements of such a source is shown schematically in Figure 17. Here, the cathode 1, the QB-semiconductor 2 and the anode 4 are concentric cylindrical layers. The QB electrons emerge into the free space FS radially and after acceleration via accelerating electrode 11, they enter the light emitting region 3 . The generated light escapes through the transparent (glass) envelope 13. Also in this arrangement, the light emitting layer 3 can be left out and the free space can be filled with the appropriate light emitting gas .

7.5. Semiconductor components and devices

The discovery of the existence, in QB-semiconductors, of quasi-ballistic electrons that can move at low applied electrical fields over macroscopic distances , as disclosed by

the present invention, will have a major impact on design and construction/manufacture of many semiconductor components and devices of both bipolar and unipolar variety. These will be used either as single units or as components/parts within Integrated Circuits' architecture. With no inelastic scattering and therefore low power dissipation, with no velocity saturation at high applied electrical fields, together with no geometrical constraints (miniaturisation of a device when fast, high frequency operation is required) on the design of the semiconductor components/devices, the present invention represents a breakthrough also in this field of application. Such ballistic or hot electron devices as they are sometimes called, have been anticipated (see for example S.M. Sze : Physics of semiconductor devices; John Wiley 1981, p. 184, but also K.W. Boer : Survey of semiconductor physics, vol.II ; Van Nostrand Reinhold 1992, p.1265 and 1247) , but the proposed structures are costly to produce and unreliable, requiring extremely small dimensions (of the order of one hundred Angstroms) and high electrical fields. The simplicity of design, robustness, relatively low cost, high reliability and long life-time of the said components based on the present invention offer a solution to all these shortcomings.

In what follows, only a brief description of some typical applications of the present invention within the field of semiconductor components, devices and Integrated Circuits' manufacture will be given and these must be considered only as few illustrative examples and in no way should they represent a limiting factor as far as the use of the present invention within this field is concerned.

The examples to be shown, have been chosen from four different major classes of semiconducting components/devices . where the present invention can be used:

Class 1 : Rectification and charge(information) storage

(Example 7.5.1 - Quasi-ballistic Schottky diode).

Other semiconductor components/devices in this class include bipolar p - n, p - i - n diodes, thyristors as well as a number of unipolar devices such as MIS (Metal - Insulator - Semiconductor) diodes, CCD (Charge - Coupled Devices), MIS tunnel diodes, MIS switch diodes, IMPATT (Impact Ionisation Avalanche Transit Time) and BARITT (Barrier Injection and Transit Time) diodes and other related Transit Time devices .

Class 2 : Photo-Sensing and Photo-Emitting devices

(Example 7.5.2. - Quasi-ballistic Photodiode and Quasi-ballistic Light emitting diode)

This class of semiconducting components/devices include among others LEDs' (Light Emitting Diodes), Photodiodes, Semiconducting Lasers, Avalanche diodes and other photoconducting devices for light to electrical signal conversion purposes.

Class 3 : Amplification and Non-volatile memory

(Example 7.5.3. - Quasi-ballistic Transistor)

Applications of the present invention in this class of semiconductor components/devices include also bipolar transistors and bipolar unijunction transistors, together with a number of unipolar components and devices inclusive FETs (Field Effect Transistor), JFETs (Junction Field Effect Transistor), MESFETs (Metal - Semiconductor Field Effect Transistor), MOSFETs (Metal - Oxide - Semiconductor Field Effect Transistor) and Non-Volatile Memory devices. Particularly relevant in relation to present invention within this class are tunnel transistors, TEDs (Transferred - Electron Devices) and all the other ballistic (Hot Electron) transistors and/or devices.

Class 4 : Optical image detection, formation and processing

Due to two-dimensional nature of the present invention, large area optical signal detection, conversion and processing is possible. Taking electromagnetic radiation as an example, the present invention can be used in a number of ways:

1. Conversion of two-dimensional optical images to electrical signals (Quasi-ballistic semiconductor camera)

2. Conversion of recorded electrical signals (electrically recorded optical images) back to two-dimensional optical images (Quasi-ballistic semiconductor Field-Emission Flat Panel Display - see also chapter 7.2.)

3. Two-dimensional optical image detection, the resulting electrical signal amplification, followed by two-dimensional optical image spatial magnification and final two-dimensional optical image recording. The result of this type of optical image processing is the original two-dimensional optical image, but now contrast/intensity amplified and spatially magnified.

In the examples to follow, the basic structure of the present invention, namely the cathode, QB-semiconductor and the anode is preserved, although in some applications only the properties of quasi-ballistic electrons between the two electrodes (the name "cathode" and "anode" will not be always used now in attempt to use more the terminology of Semiconductor Physics) are utilised rather than their ability to escape from the basic structure into free space FS (see Figure 2). These properties are very similar to the properties of electrons moving between a cathode and an anode in a vacuum tube, only now no vacuum is needed, the injection of electrons from the cathode takes place at room temperature and the whole device in question can be made of submicron dimensions. In this way the present invention combines all the advantages of vacuum

tubes and modern all solid state semiconductor device technology/design/construction.

7.5.1. Quasi-ballistic Schottky barrier diode

Figure 18 is a schematic diagram of a typical, fast, planar Schottky barrier diode, together with the equivalent R , C electrical network (according to the US patent n.: 5 627 479 and European patent n.: EP 0 672 257 B1 by one of the authors of the present invention), describing the electrical response of such a diode in the prior art (SEM in Figure 18) and according to the present invention (QB-Sem in Figure 18). In reference to Figure 18 now, the diode current "Idiode" is controlled by the depletion resistance Rd which is in turn determined by the extend of the depletion region Wd . This depletion region length (width) Wd is exponentially dependent on the applied voltage Vso between the Schottky and Ohmic electrical contacts. The rectification action is achieved through the control of Wd by Vso which in turn induces exponentially strong changes in Rd that controls the diode current "Idiode" (forward and reverse diode current). In high frequency applications it is necessary to diminish the over-all dimension L and in particular the distance Lso between the front of the depletion region and the ohmic contact.

Using the present invention (substitution of SEM material by QB-Sem material in Figure 18) , this geometrical constrain is not necessary. The Quasi-ballistic Schottky diode according to the present invention will be not only workable at higher frequencies (no electron velocity saturation at high electrical fields), but it will be characterised by simpler design and very low power dissipation through shunting of the resistor Rqb-sem by Lqb (quasi-ballistic electrons' kinetic inductance) as shown in Figure 18 .

7.5.2. Quasi-ballistic Photodiode and Quasi-ballistic Light-Emitting Diode

A simplified energy band diagram shown in Figure 19 illustrates the physical principles behind and one possible construction (preferred embodiment) of a quasi-ballistic photodiode (device 1), a quasi-ballistic Light-Emitting diode (device 2) and one of the possible constructions (preferred embodiment) of a first stage of an optical signal detection/amplification/spatial magnification device (device 3), all according to the present invention. These devices will be now discussed in turn.

Quasi-ballistic photodiode (process 1 in Figure 19)

The optical signal (incoming light) is absorbed within the cathode region (region between the surfaces S1 and S2 - Figure 19) and a thin region within the QB-semiconductor that lies close to the surface S2 , creating in this process a number of electron - hole pairs (process marked "Exc1" in Figure 19). The photo-excited electrons then constitute the quasi-ballistic current "Ibal", are accelerated and enter the avalanche multiplication region AMR through the surface S5. The avalanche multiplication process AM leads to an amplified electrical current signal "Ie" and "Ih". In some applications the avalanche multiplication region AMR can be left out, the electrical signal from the photon - electron conversion ("Exc1") being sufficiently amplified through the acceleration of the generated quasi-ballistic electrons.

The described quasi-ballistic photodiode according to the present invention has high quantum efficiency, relatively very low power dissipation and can be manufactured in a form of two-dimensional photo-sensor array when two-dimensional optical image (signal) detection and processing is required .

Quasi-ballistic Light-Emitting Diode (process 2 in Figure 19)

In the case of Light-Emitting device, the electrical signal (voltage bias between the cathode and the anode) that can be also time modulated if needed (opto-electronic applications) , controls the amount of injected electrons that enter the QB-semiconductor region QB-Sem (process "Exc2" in Figure 19) . After acceleration, while moving through the QB-Sem region , these electrons (current "Ibal" in Figure 19) enter the Light Emitting Region LER through the surface S5 and create photon flux through the process of recombination across the band gap Eg (see Figure 2 and process 2 in Figure 19). This photon flux (that is also time modulated if the cathode - anode voltage bias ~ $\Delta Q(t)$ is time dependent) then finally emerges into the free space FS .

When the electron injection process "Exc2" is of sufficient intensity and the light emitting region LER (normally heavily p-doped) satisfies the necessary conditions for population inversion, the above described device will function as a quasi-ballistic semiconductor laser with a very low power dissipation, high efficiency and can be used very effectively in opto - electronic applications such as optical fibre signal transmission and tele-communications in general .

Optical image detection and processing (process 3 in Figure 19)

In some applications it will be necessary and/or advantageous to process the quasi-ballistic current "Ibal" , formed either through process "Exc1" and/or through process "Exc2", electron - optically . In this case the region between the interface S5 and S3 is just a continuation of the quasi-ballistic semiconductor region QB-Sem as shown in Figure 19 . After traversing the anode region, these quasi-ballistic electrons emerge through the surface S4 into hte free space FS as the electron emission current "Iem" which can be now

processed electron - optically . A device of this type will described in 7.5.4. .

7.5.3. Quasi-ballistic Transistor

Figure 20 is a schematic diagram of a typical planar Metal - Semiconductor Field Effect Transistor (MESFET). The current "Id" between the source and the drain electrodes is controlled by the voltage "Vg" through changing the active depletion width "Wd (Vd)". "a" is the electrically active part of the substrate semiconductor SEM, "L" is the conductivity channel length and "Z" is the width of the device . When a high speed performance is required , the channel length has to sufficiently reduced (< 1.5 micron) and the typical operating voltages "Vds" create high electrical fields between the source and the drain . The velocity of electrical charges (electrons) becomes then saturated (electrical field dependent mobility region is reached) and this limits the speed of the said device operation.

Now, even if the geometrical design of the said MESFET transistor as shown in Figure 20 is kept the same for the sake of simplicity and clarity of the argument, the two above mentioned design constraints (small geometry and electron velocity saturation) are non-existent, when such a MESFET transistor is constructed according to the present invention . Given the form of the device as shown in Figure 20, this involves simple replacement of the standard semiconductor substrate SEM (see Figure 20) by the quasi-ballistic semiconductor QB-Sem .

MESFET device according to the present invention and depicted in Figure 20 is characterised not only by fast response (high frequency response) , but also by very low power dissipation since source-drain current Id is quasi-ballistic in nature .

It has to stressed at this point again that the design structure of MESFET transistor shown in Figure 20 is only one of a large number of possible designs of an amplification / switching device. Due to the nature of the present invention, other more optimal designs are possible and will be realised . These will take over some design features from vacuum tubes (see for example the above mentioned publication by K.W. Boer : p.1237) .

The same and/or very similar arguments as discussed above for the case of MESFET transistor lie behind the construction of Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET), Non-Volatile memory MOSFETs and other devices within this class according to the present invention . All of these devices are characterised by simplicity of design, robustness, high response speed and very low power dissipation.

7.5.4. Optical image detection, formation and processing

(Two-Dimensional Detector arrays of electromagnetic radiation)

As mentioned in the introductory remarks to this chapter (chapter 7.5. - Semiconductor components and devices), the class 4 (7.5.4. Optical image detection, formation and processing) involves what could be roughly defined as three basic applications of the present invention :

1. Quasi-ballistic semiconductor camera
   (Conversion of 2D-optical images/signals to electrical signals)
2. Quasi-ballistic semiconductor Field-Emission Flat Panel Display
   (Conversion of electrical signals to 2D-optical images/signals)
3. A system for 2D-optical image/signal brightness/contrast amplification and spatial magnification

In this paragraph a short description of QB-semiconductor camera and of optical image/signal processing system will be described , while QB-semiconductor Field-Emission Flat Panel Display has been already dealt with in chapter 7.2.

For the sake of clarity and simplicity, the two applications will be described assuming the optical signal to be in the form of two-dimensional optical image formed by the photons from within the visible part of the electromagnetic radiation spectrum. This of course must not be considered in no way as a limiting factor in relation to the present invention and its use within this class of applications. The optical signal to be detected/processed may well be from within other parts of the electromagnetic radiation spectrum and/or it may be a signal formed by other particles. The optical image spatial dimension can also vary from zero to three.

Finally, the specificity of the two application examples of the present invention to be presented below, serves purely illustrative/pedagogical purposes and must not be considered either as a limiting factor in relation to the applications of the present invention within this field.

<u>Quasi-ballistic semiconductor camera</u>

(Conversion of two-dimensional (2D) optical images to electrical signal sequences)

Figure 21 is a schematic diagram of a device according to the present invention for the detection and recording of two-dimensional optical signals/images. In this preferred embodiment the QB-semiconductor is sandwiched between a cathode 1 and an anode 4 . Both electrodes are patterned in a way similar to x , y patterning shown in Figure 5 . The metal cathode, QB-semiconductor and the anode form a two-dimensional array of Schottky barrier photodiodes that can be addressed

individually and sequentially, as illustrated in Figure 5 (pixel diode i , j - switched on) .

The optical image is formed at around the surface S2 and is transformed and processed , with help of the said device, to time sequence of electrical signals in the following way :

Optical image forming light (photons) enters the said structure shown in Figure 21 through appropriate colour filters R(red), Y(yellow) and B(blue) and it is absorbed within the region consisting of cathode - QB-semiconductor interface and QB-semiconductor depletion region, creating in this process a number of electron - hole pairs .

By "switching-on" a particular pixel diode (i , j) by applying an appropriate electrical voltage between a cathode strip "i" and an anode strip "j" (diode with yellow colour filter "Y" in Figure 21), the created quasi-ballistic electrons are accelerated within the QB-semiconductor region QB-Sem (Figure 21) and if needed can be amplified further by avalanche multiplication within the avalanche multiplication region AMR (Figure 21) . The resulting current pulse then forms the electrical signal which is related to the light intensity of "yellow" photons impinging on the pixel (i, j) shown in Figure 21.

The overall thickness (Dim2) of the said device (QB-semiconductor camera) is in the region of few millimetres, while the active area of the said device (lateral dimension Dim1) can be of the order of up to some 30 centimetres with the present day technology. High quantum efficiency, high spatial resolution, robustness and the simplicity of construction are just few of the attractive features of the proposed device according to the present invention .

<u>Optical signal/image processing device</u>

In a number of applications (such as astrophysics, infrared vision/imaging and others), very weak, two-dimensional optical images have to be detected, processed and recorded , with an additional demand for high spatial resolution/magnification and/or for spectral information to be extractable. One of possible devices according to the present invention that fulfils these requirements is shown schematically in Figure 22. It consists of two parts, where part A is the two-dimensional optical image/signal amplification part, while the part B is the two-dimensional optical image/signal spatial magnification part .

The incoming electromagnetic radiation that forms the optical image in the plane of the primary optical image (see Figure 22) is absorbed within the region of the cathode, interface S2 and the depletion region of the QB-semiconductor as indicated schematically in Figure 22 , creating in this way a number of electron - hole pairs . This number depends both on the energy of incoming photons (spectroscopic information) and on the number of incoming photons (the signal intensity information). The quasi-ballistic electrons created within the plane of the primary optical image are accelerated within the QB-semiconductor region QB-Sem (Figure 22) (primary amplification) and because of their properties they can leave the basic planar electron emitter structure (cathode, QB-semiconductor and the anode) through the surface S4 . At the same time though they form in this way also an electron - optical image of the original optical image in the plane of the primary optical image. This is shown schematically in Figure 22 by one to one correspondence between the point "i" in the plane of the primary optical image and the point "i" in the plane of the surface S4 .

After this photon to electron conversion (photon in - electron-hole pair out) and primary amplification (acceleration of the created electrons within QB-Sem region), the obtained electron-optical image formed in the plane of the surface S4

can be processed further by suitable electron optics . It is further amplified with the help of the accelerating electrode (secondary amplification) and can be if needed spatially magnified (electron-optical primary spatial magnification) .

This spatially magnified and intensity amplified electron-optical image is converted back to a second stage optical image with the help of an appropriate electron scintilator as indicated in Figure 22 . The plane of this second stage optical image then becomes the object plane of the final optical magnification system to secure the secondary spatial magnification of the original optical image. The final optical image, that is signal/intensity amplified and spatially magnified is then formed in the plane of the final optical image ready for recording purposes . Depending on the spatial resolution required, the whole assembly (part A and part B) can be moved laterally within the plane of the primary optical image.

Finally it should be pointed out that because of the characteristic properties of the basic planar electron emitter that forms the bottom portion of the part A of the device shown in Figure 22, the said planar electron emitter in conjunction with the electron-optical parts within the free space region FS can be used as a spectroscopic device, extracting the necessary information about the photon energy spectrum within the primary optical image.

7.6. Photovoltaic applications

Due to a very low inelastic scattering and recombination rates of the quasi-ballistic electrons, a Schottky barrier diode according to the present invention is a highly efficient photoconductor and its use in the photovoltaic applications is obvious . One of the possible constructions of a solar cell

according to the present invention is shown schematically in Figure 23.

The said device is formed by QB-semiconductor layer sandwiched between two electrodes - a cathode (Metal1) and an anode (Metal2). While the cathode and the QB-semiconductor form a Schottky rectifying contact, the anode and the QB-semiconductor form an ohmic contact. When constructed in this way, the internal electrical field E (x) within the said device, caused by the electrical charge transfer that takes place in order to establish thermodynamical equilibrium, has a profile shown in the bottom part of Figure 23.

The sun light enters the said device (solar cell according to the present invention) from the right (Figure 23) through the cathode and is absorbed within the structure, creating single electron-hole pair per incoming photon . Three, spatially separated absorption processes can be distinguished . The process 1 is the generation of electron-hole pair at the interface between the cathode and the QB-semiconductor. The process 2 is a generation of electron-hole pair within the depletion region of the QB-semiconductor and finally the process 3 describes the photon absorption process generating electron-hole pair within the bulk of the QB-semiconductor (region of QB-Sem where the internal electrical field is zero) . Due to the existence of quasi-ballistic trajectories within the QB-semiconductor a majority of electrons generated especially within the depletion region of the QB-semiconductor will be accelerated by the internal electrical field existing within the depletion region Wd towards the anode without recombination and/or inelastic scattering. This effect increases appreciably the quantum efficiency of the said solar cell. By optimising the structure of the said device through minimising the extend of the bulk region and through an appropriate choice of the cathode material (transparent conducting tin oxide for example), the solar cell according to the present invention represents a very efficient, simple and

robust light to electricity energy conversion device with a large active area.

7.7. Electron Emission Microscopy

There is a potentially very important application of the present invention within the field of defects and/or imperfections investigations in the "virgin" semiconductor wafers by what is termed here as Electron Cold Emission Microscopy (ECEM). In the standard version of the Electron Emission Microscopy, a sample to be investigated is heated up to temperatures when the thermal electron emission becomes finite . These electrons leave the surface S3 (Figure 24) and are subsequently electron-optically processed to form a high spatial resolution electron optical image of that fraction of the surface S3 through which they emerged into the vacuum. The information about the sample under investigation that can be extracted from such type of electron microscopy is though limited to the surface S3 and few monolayers of the material right below it. This is because under these conditions the mean free path of the electrons (with sufficient energies to escape into vacuum) is extremely small (well below some 50 Angstroms).

In the proposed version of this experimental method according to the present invention, the electrons that leave the sample (QB-Sem region in Figure 24) through the surface S3, have been injected to the said QB-semiconductor already at the surface S2 and therefore they carry the information about the conditions of the sample along the whole of their quasi-ballistic trajectory within the sample. Any imperfections and/or defects (these may be of one, two and/or three - dimensional variety) will cause their scattering (and their subsequent thermalising) away from their quasi-ballistic straight trajectories. This creates a projection-type of contrast in the electron-optical image plane.

One of the possible preferred embodiments of the said Electron Cold Emission Microscopy according to the present invention is shown schematically in Figure 24. The basic structure of the present invention (cathode, QB-semiconductor, anode - see also Figures 1 and 2) is preserved also in this case, only now the said basic structure forms a sample to be investigated. Furthermore, as has been already explained in chapter 7.1., the metal electrodes facing the QB-semiconductor surface S2 and S3 are not really necessary, provided that the electrical field of sufficient strength can be generated within QB-semiconductor body and the electrons can be injected into the QB-semiconductor through the surface S2. In such configuration the whole process of virgin defect quality control can be performed contactless ! These injected electrons travel along their straight, quasi-ballistic trajectories and those not deflected by imperfections, impurities, defects and/or other irregularities, will eventually emerge into vacuum through the surface S3 of the QB-semiconductor. The surface density of these electrons, their energies and the angle of their emergence are the parameters (quantities) that are related to the precise quasi-ballistic electrons' interaction with the surface S2, with the bulk of the QB-semiconductor along their trajectory and with the surface S3.

The electrons emerging through the segment "Sseg" (Figure 24) of the surface S3 are then processed by standard electron optics to form high spatial resolution (magnified) electron-optical image of the said segment "Sseg" in the electron-optical image plane (see Figure 24) .

By placing the QB-semiconductor on a high precision x , y stage, the whole wafer can be investigated in this way down to 10 to 50 Angstroms standard resolution of a typical scanning electron microscope.

7.8. Electron beam sources in general

Although the present invention (planar electron emitter) is primarily targeted towards applications that require and/or benefit from the two-dimensional nature of the said invention, the present invention characteristics (such as low power dissipation, simplicity of construction, high electron emission current density and room temperature operation) make the use of the present invention in the construction of more standard electron beam sources also very attractive. Pointed, patterned, quasi-planar and general shape electron sources can be manufactured with ease and are termed here as "Cold Schottky Cathodes". Their typical use will be as electron sources for Cathode Ray Tubes (CRT), x-ray tubes, Electron microscopes inclusive electron guns for evaporation, welding, imaging and possibly other electron beam applications.

Since all these applications are considered as trivial use the present invention and because they are well known and scribed in the corresponding prior art, they will not be scussed here in more detail.

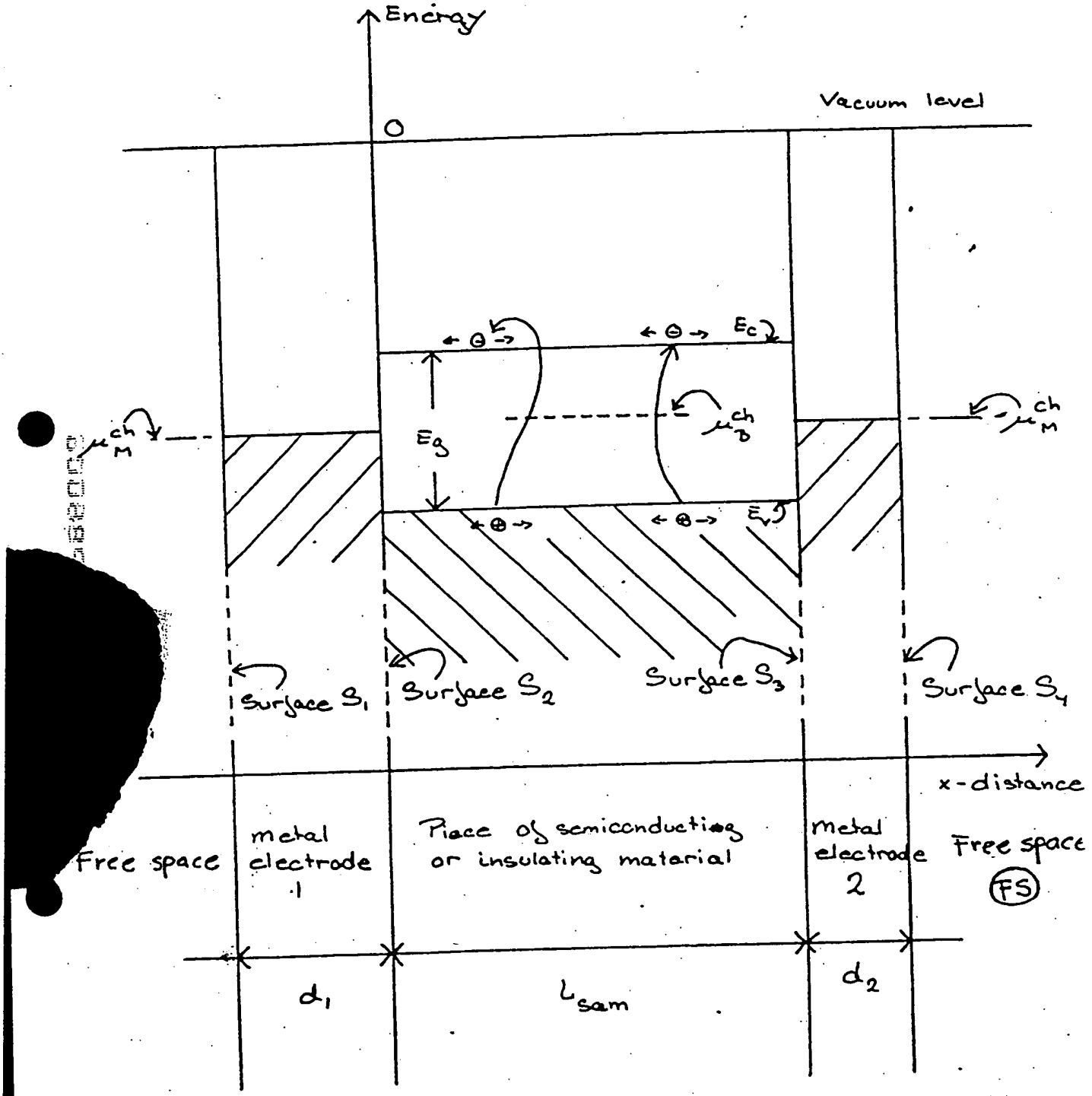
Energy
Vacuum level
0
E_c
E_g
E_v
μ^{ch}_M
μ^{ch}_D
μ^{ch}_M
Surface S_1
Surface S_2
Surface S_3
Surface S_4
x-distance
Free space
metal electrode 1
Piece of semiconducting or insulating material
metal electrode 2
Free space
FS
d_1
L_{sam}
d_2

FIGURE 1

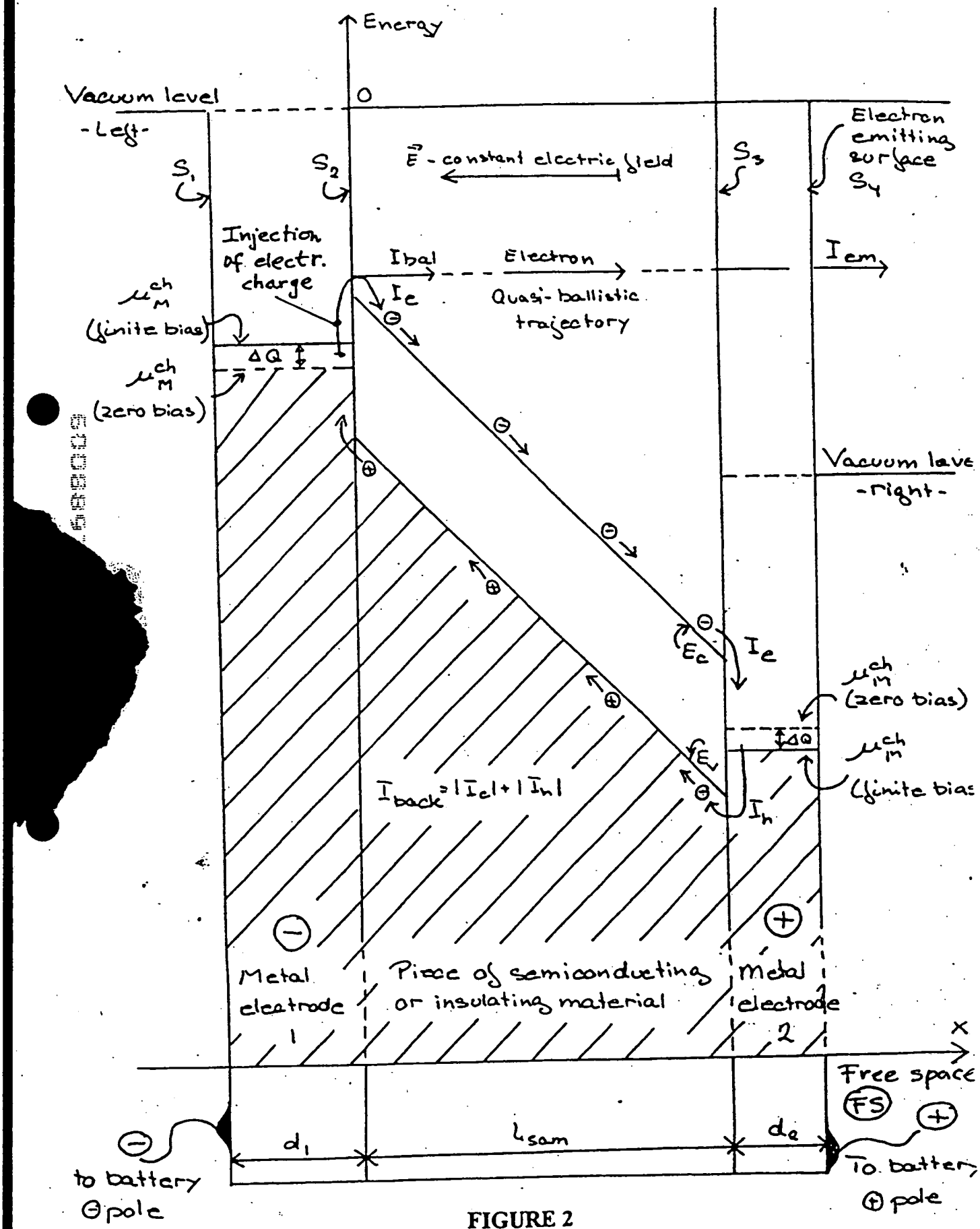
Energy
Vacuum level
- Left -
0
S_1
S_2
$\vec{E}$ - constant electric field
S_3
Electron emitting surface S_4
Injection of electr. charge
Ibal
Electron
Quasi-ballistic trajectory
I_{em}
μ_M^{ch} (finite bias)
ΔQ
μ_M^{ch} (zero bias)
I_e
Vacuum level
- right -
E_c
μ_m^{ch} (zero bias)
ΔQ
μ_m^{ch} (finite bias)
E_v
$I_{back} = |I_e| + |I_h|$
I_h
Metal electrode 1
Piece of semiconducting or insulating material
Metal electrode 2
x
Free space
FS
d_1
L_{sam}
d_e
to battery ⊖ pole
To battery ⊕ pole

FIGURE 2

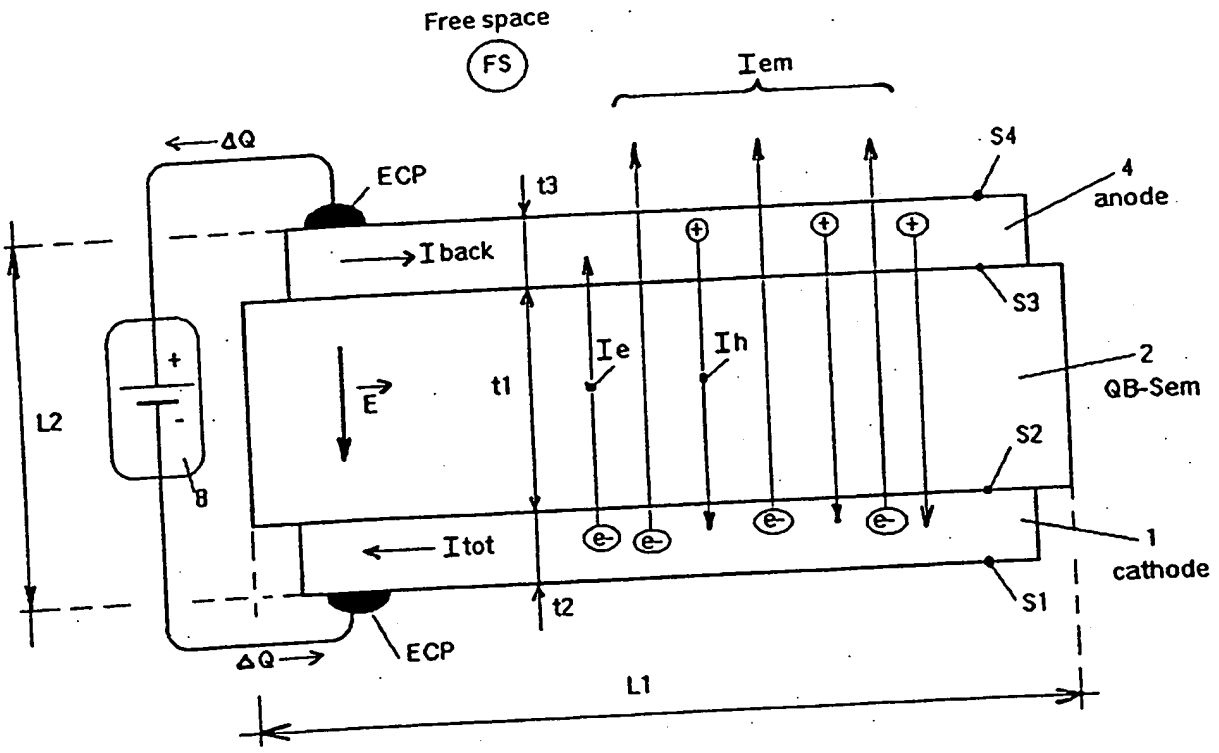
Free space
FS
Iem
ΔQ
ECP
t3
S4
4
anode
Iback
S3
2
QB-Sem
Ie
Ih
E
t1
L2
S2
B
Itot
1
cathode
t2
S1
ECP
ΔQ
L1

FIGURE 3

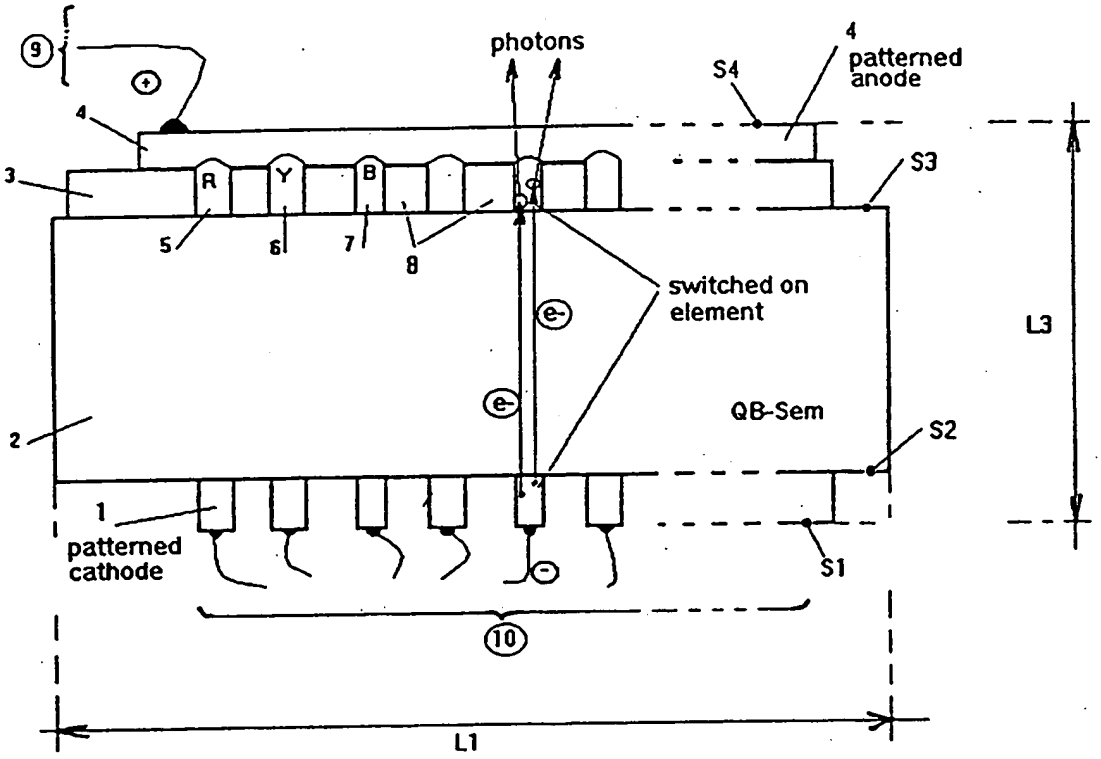
9
photons
4
patterned
anode
S4
4
3
R
Y
B
S3
5
6
7
8
switched on
element
e-
L3
e-
QB-Sem
2
S2
1
patterned
cathode
S1
10
L1

FIGURE 4

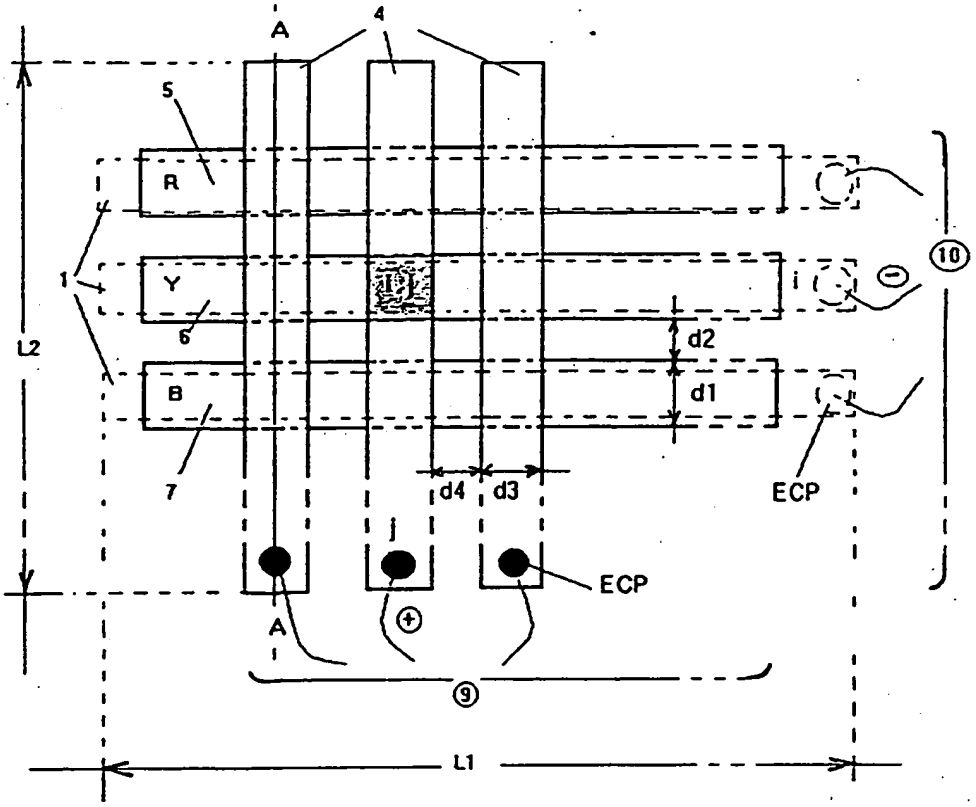

FIGURE 5

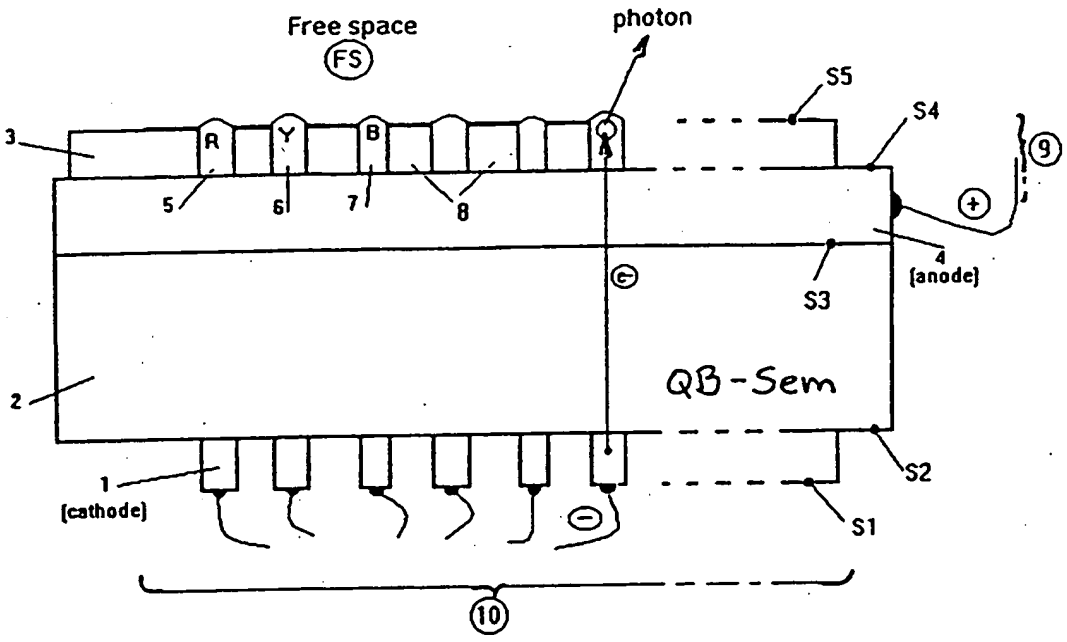
Free space
FS
photon
S5
S4
9
3
R
Y
B
5
6
7
8
+
4
(anode)
S3
2
QB-Sem
S2
1
(cathode)
S1
10

FIGURE 6

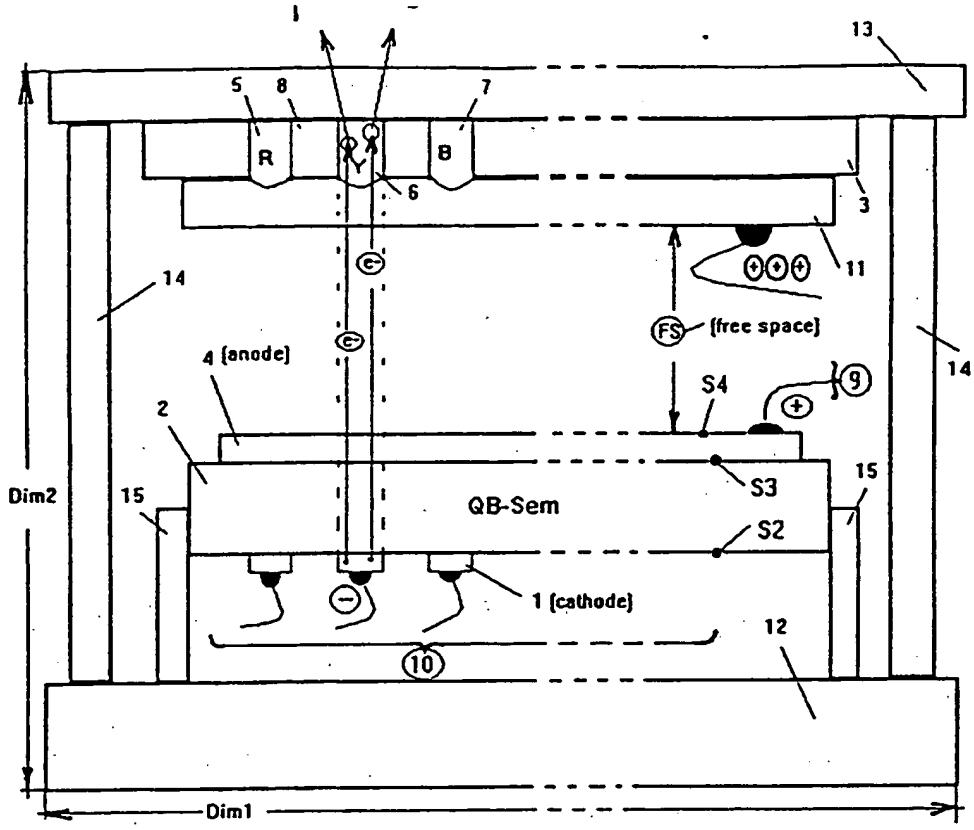
1
13
5
8
7
R
B
6
3
11
14
FS
[free space]
4 [anode]
S4
9
14
2
S3
15
Dim2
15
QB-Sem
S2
1 [cathode]
12
10
Dim1

FIGURE 7

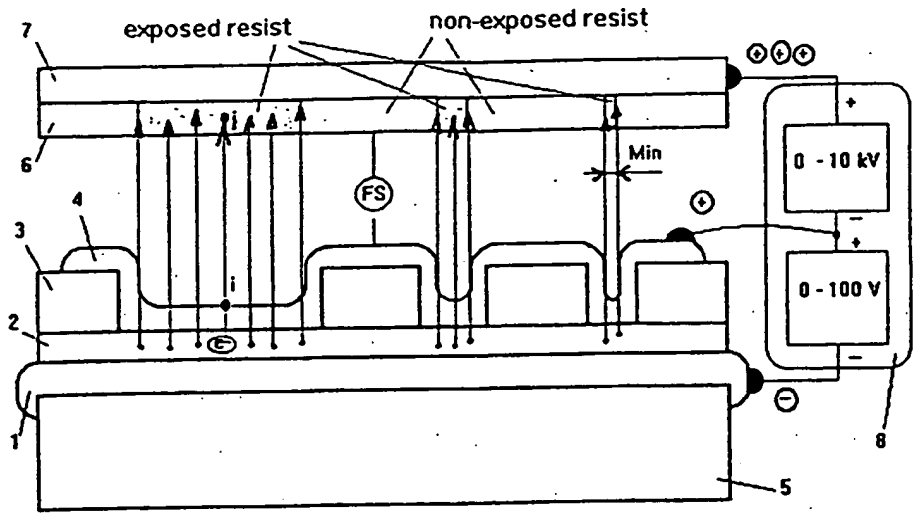
7
exposed resist
non-exposed resist
6
Min
FS
4
3
2
1
0 - 10 kV
0 - 100 V
8
5

FIGURE 8

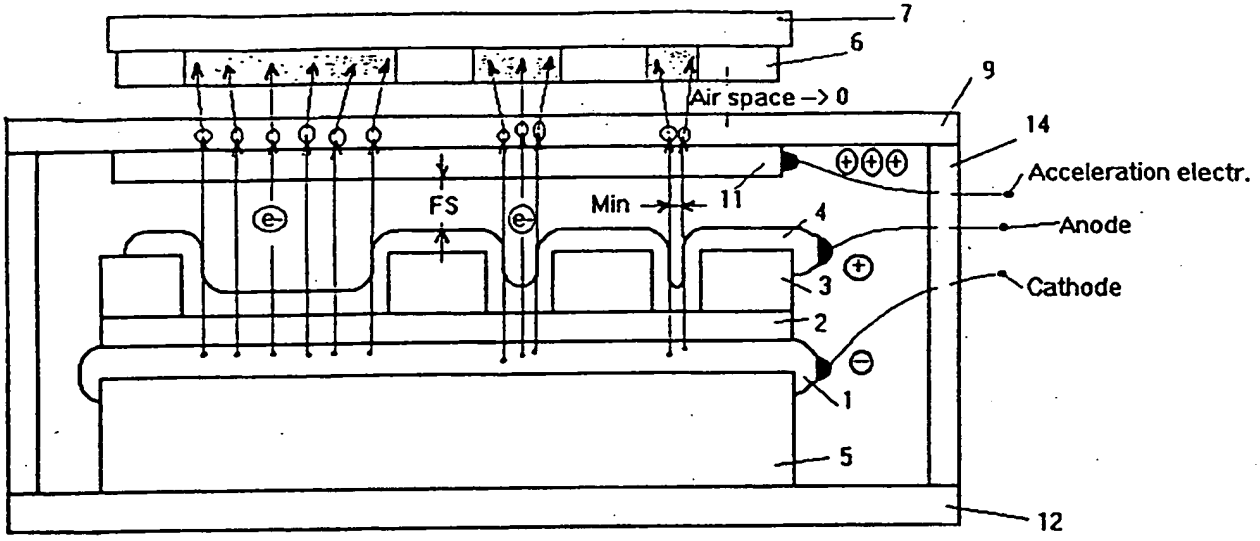
7
6
9
Air space -> 0
14
Acceleration electr.
FS
Min
11
4
Anode
3
Cathode
2
1
5
12

FIGURE 9

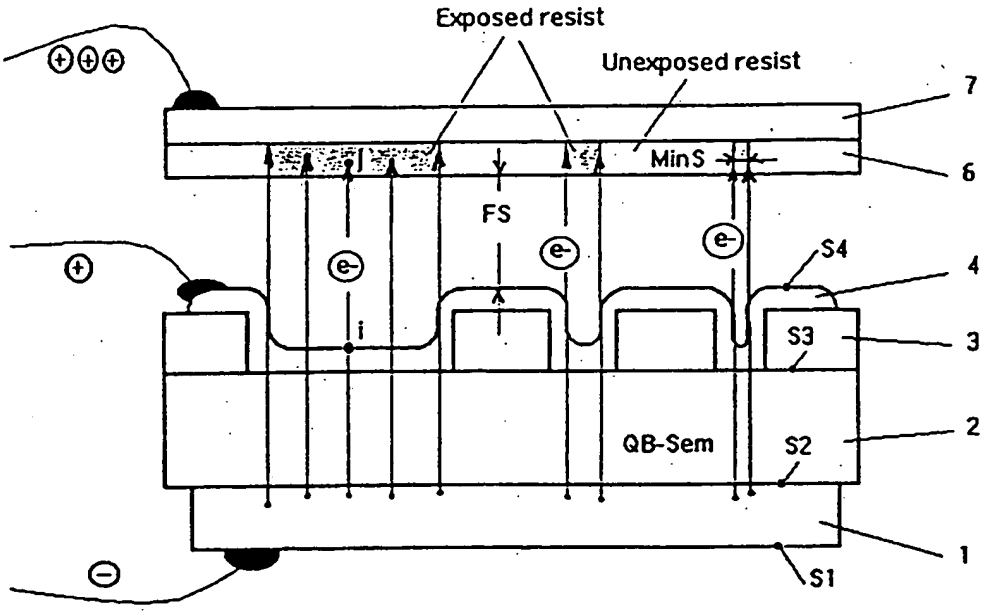
Exposed resist
Unexposed resist
7
6
MinS
FS
e-
e-
e-
S4
4
i
S3
3
QB-Sem
S2
2
1
S1

FIGURE 10

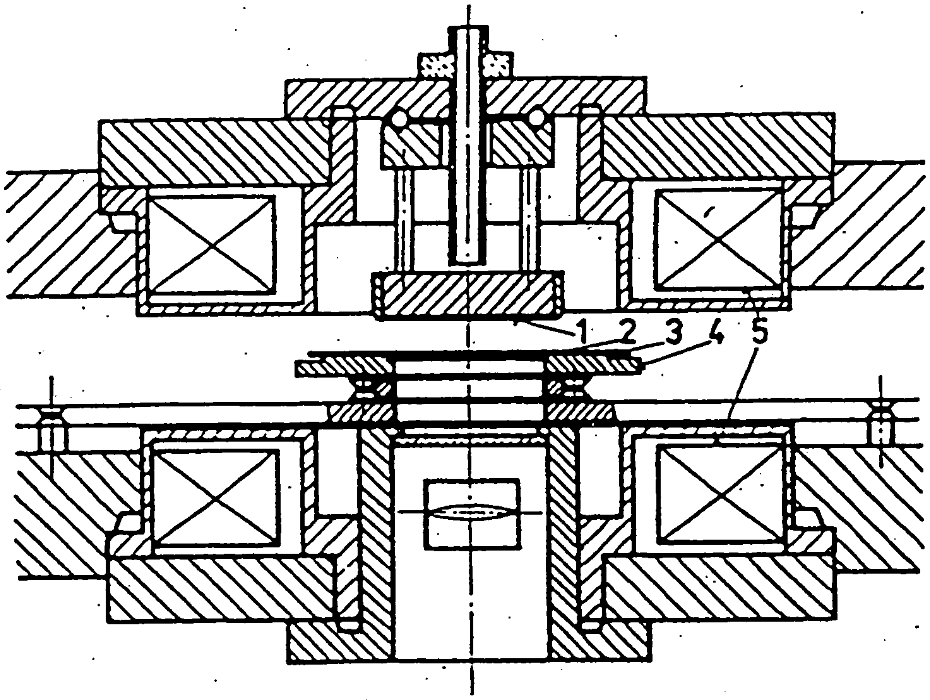

FIGURE 11

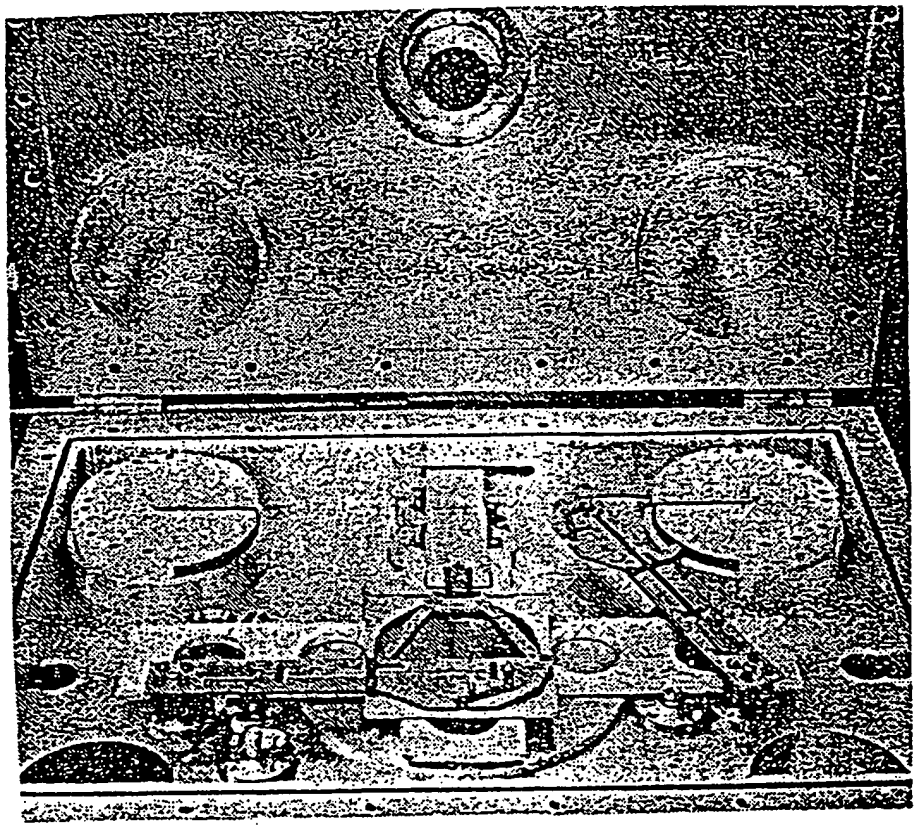

FIGURE 12

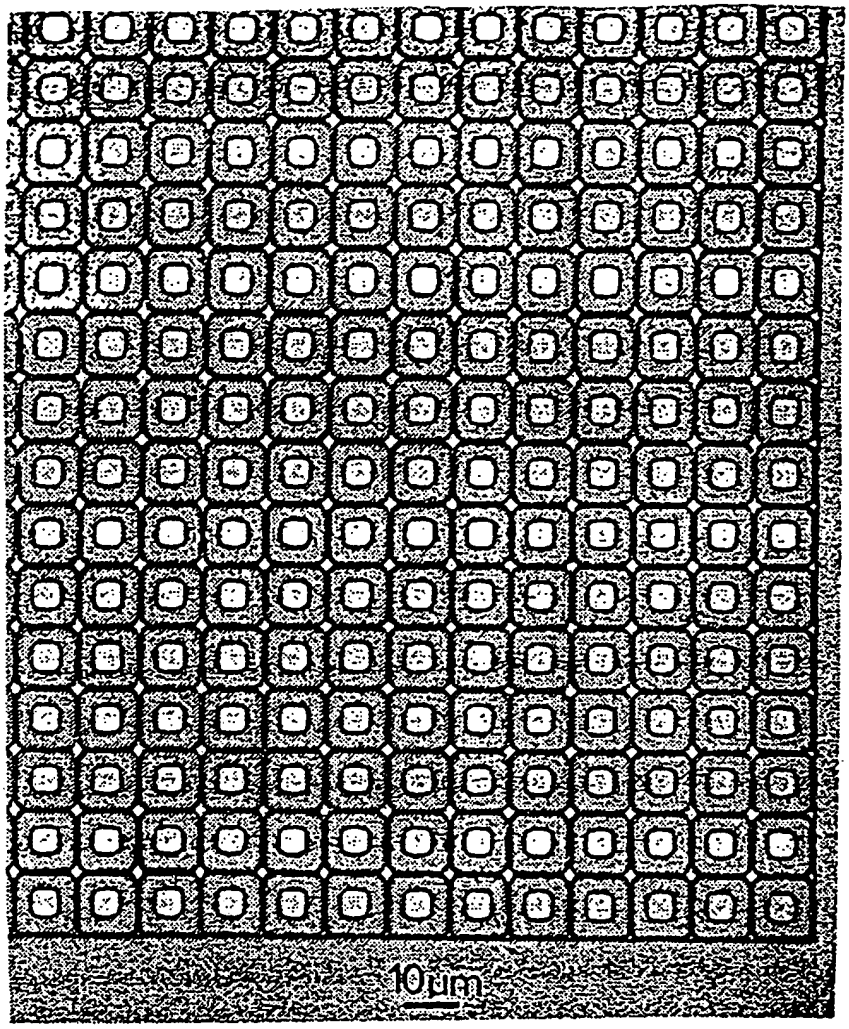

FIGURE 13

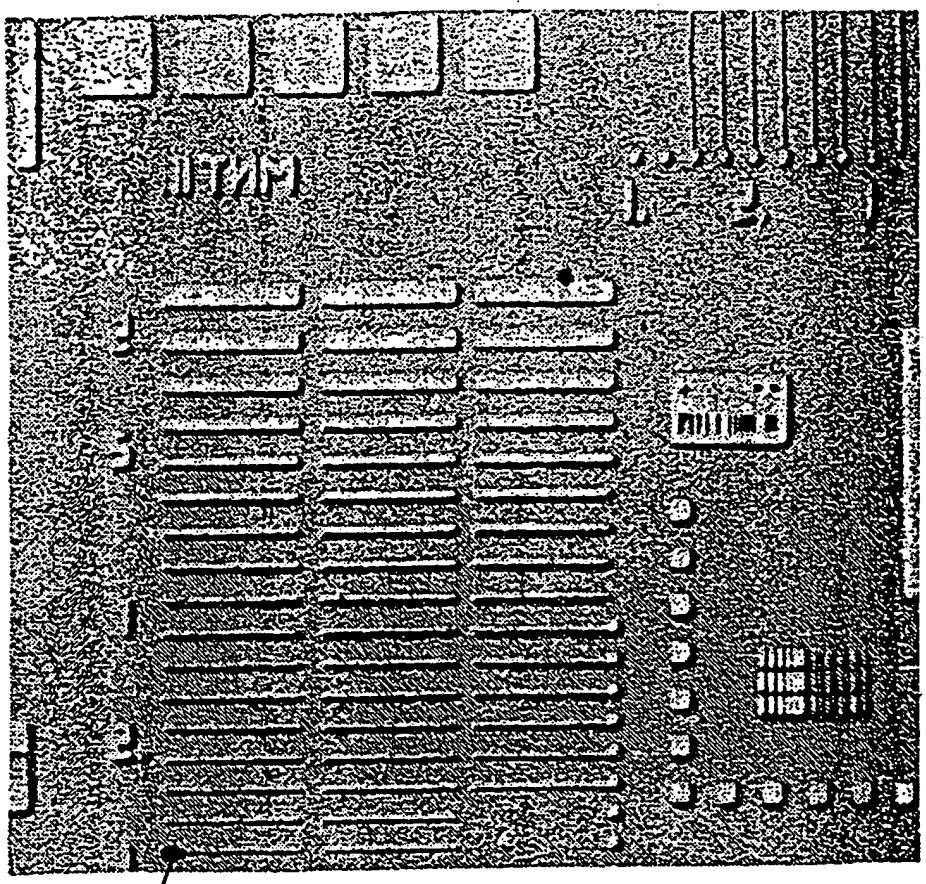

FIGURE 14

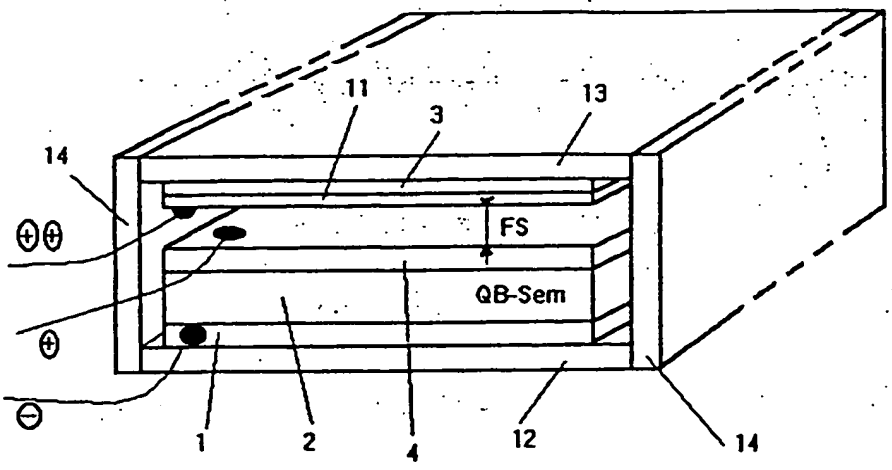

FIGURE 15

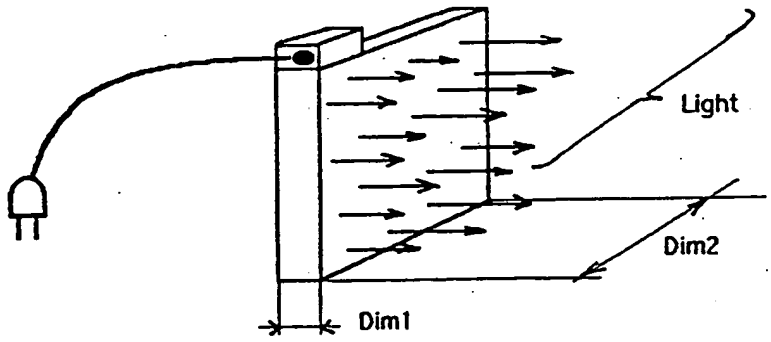

FIGURE 16

09/14/2005 08:09 #165

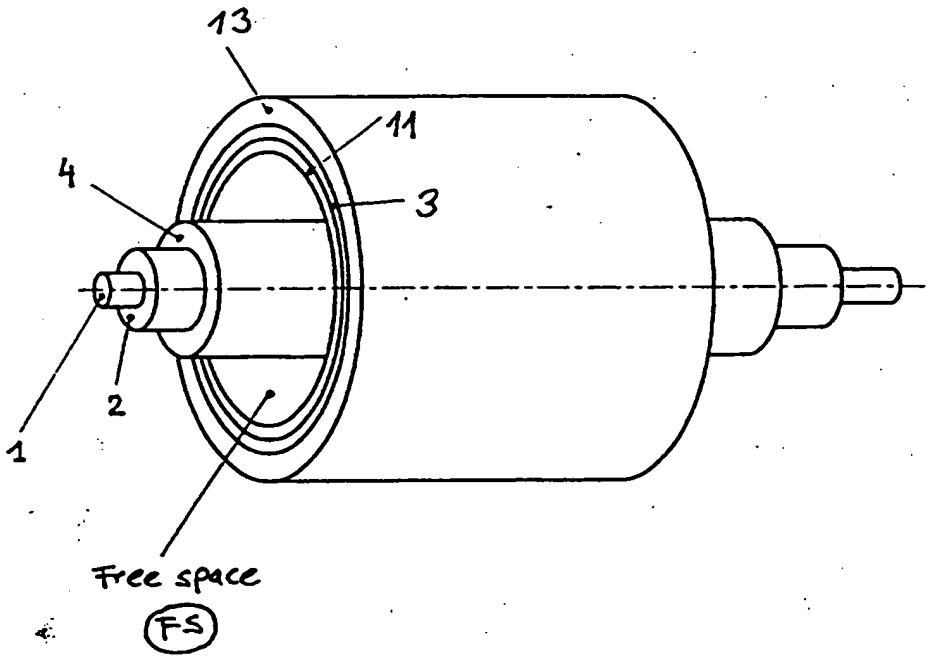

FIGURE 17

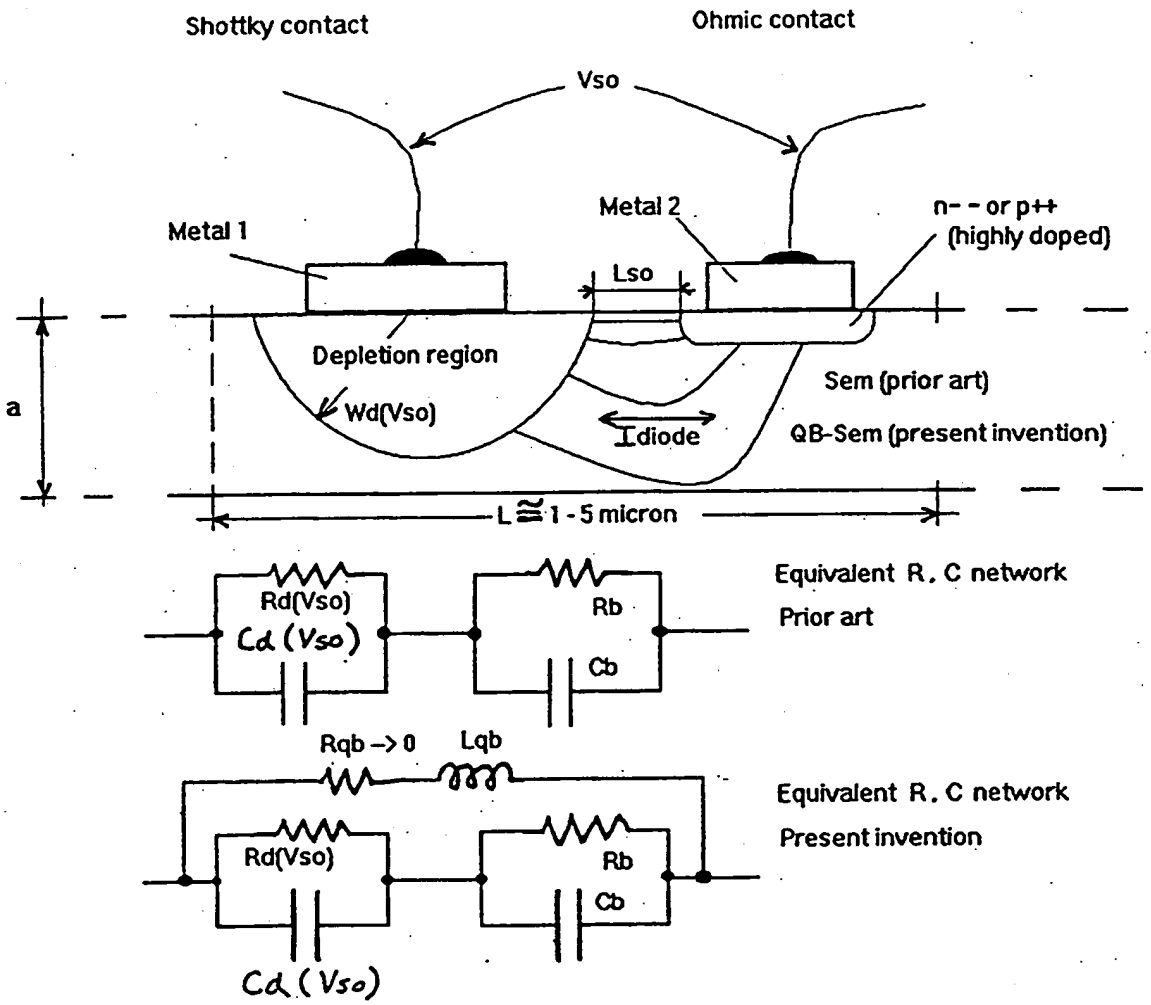
Shottky contact
Ohmic contact
Vso
Metal 1
Metal 2
n- - or p++
(highly doped)
Lso
Depletion region
Wd(Vso)
a
Idiode
Sem (prior art)
QB-Sem (present invention)
L ≅ 1 - 5 micron
Rd(Vso)
Cd (Vso)
Rb
Cb
Equivalent R, C network
Prior art
Rqb -> 0
Lqb
Rd(Vso)
Rb
Cb
Equivalent R, C network
Present invention
Cd (Vso)

FIGURE 18

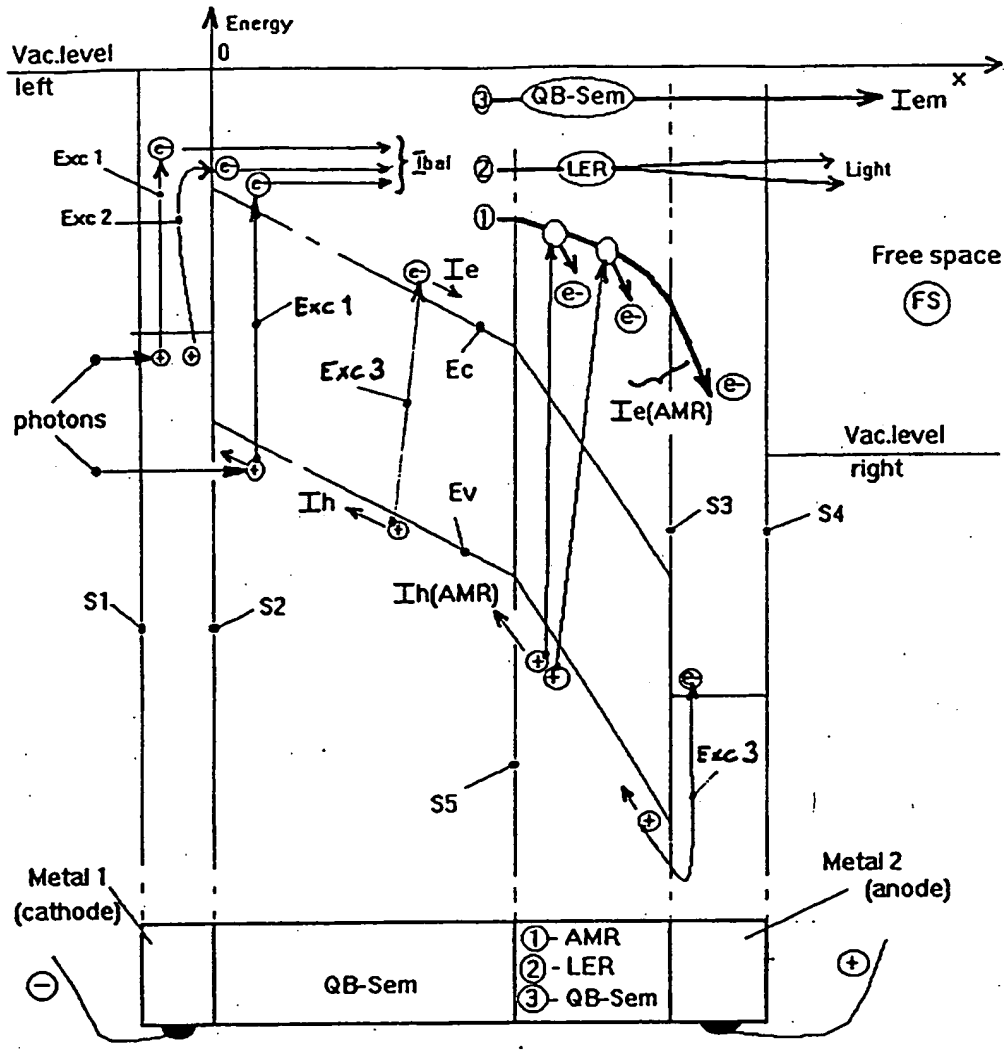
Energy
Vac.level
left
0
x
3
QB-Sem
Iem
2
LER
Light
1
Free space
FS
Exc 1
Exc 2
Ibal
Ie
Exc 1
Exc 3
Ec
Ie(AMR)
photons
Vac.level
right
Ih
Ev
S3
S4
S1
S2
Ih(AMR)
Exc 3
S5
Metal 1
(cathode)
Metal 2
(anode)
1- AMR
2- LER
3- QB-Sem
QB-Sem

FIGURE 19

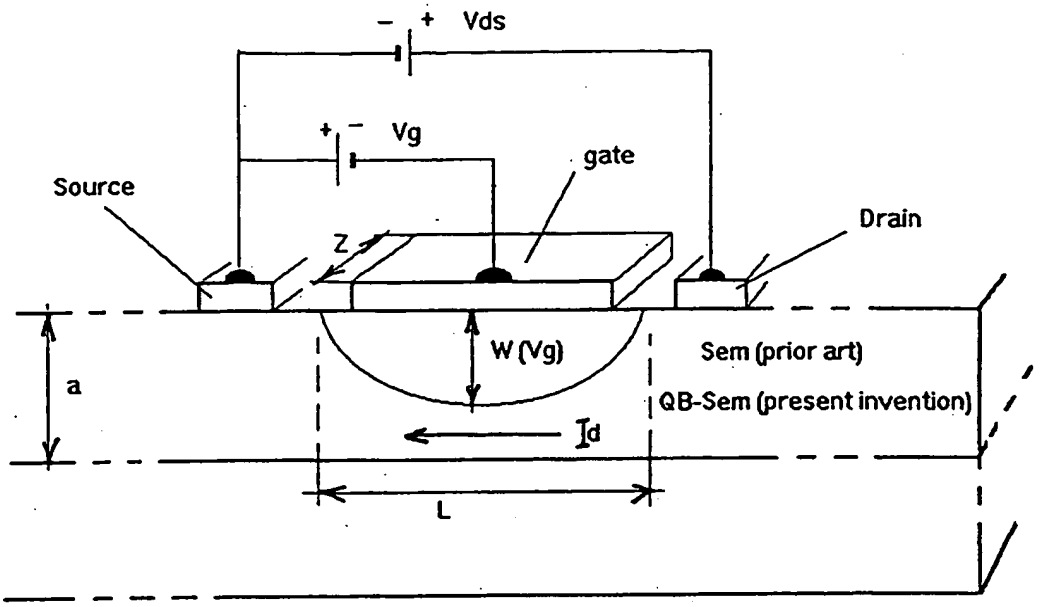
Vds
Vg
gate
Source
Drain
Z
W (Vg)
Sem (prior art)
QB-Sem (present invention)
a
Id
L

FIGURE 20

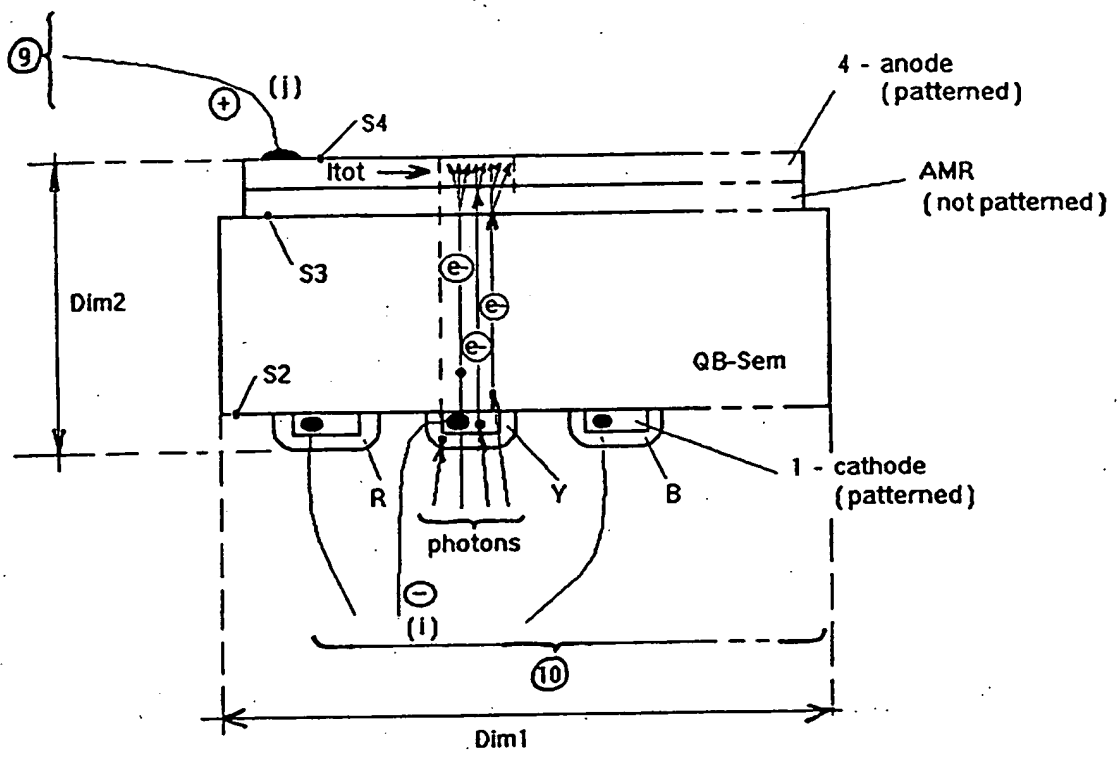
9
(+)
(i)
S4
4 - anode
(patterned)
Itot
AMR
(not patterned)
S3
Dim2
e-
e-
e-
QB-Sem
S2
1 - cathode
(patterned)
R
Y
B
photons
(-)
(i)
10
Dim1

FIGURE 21

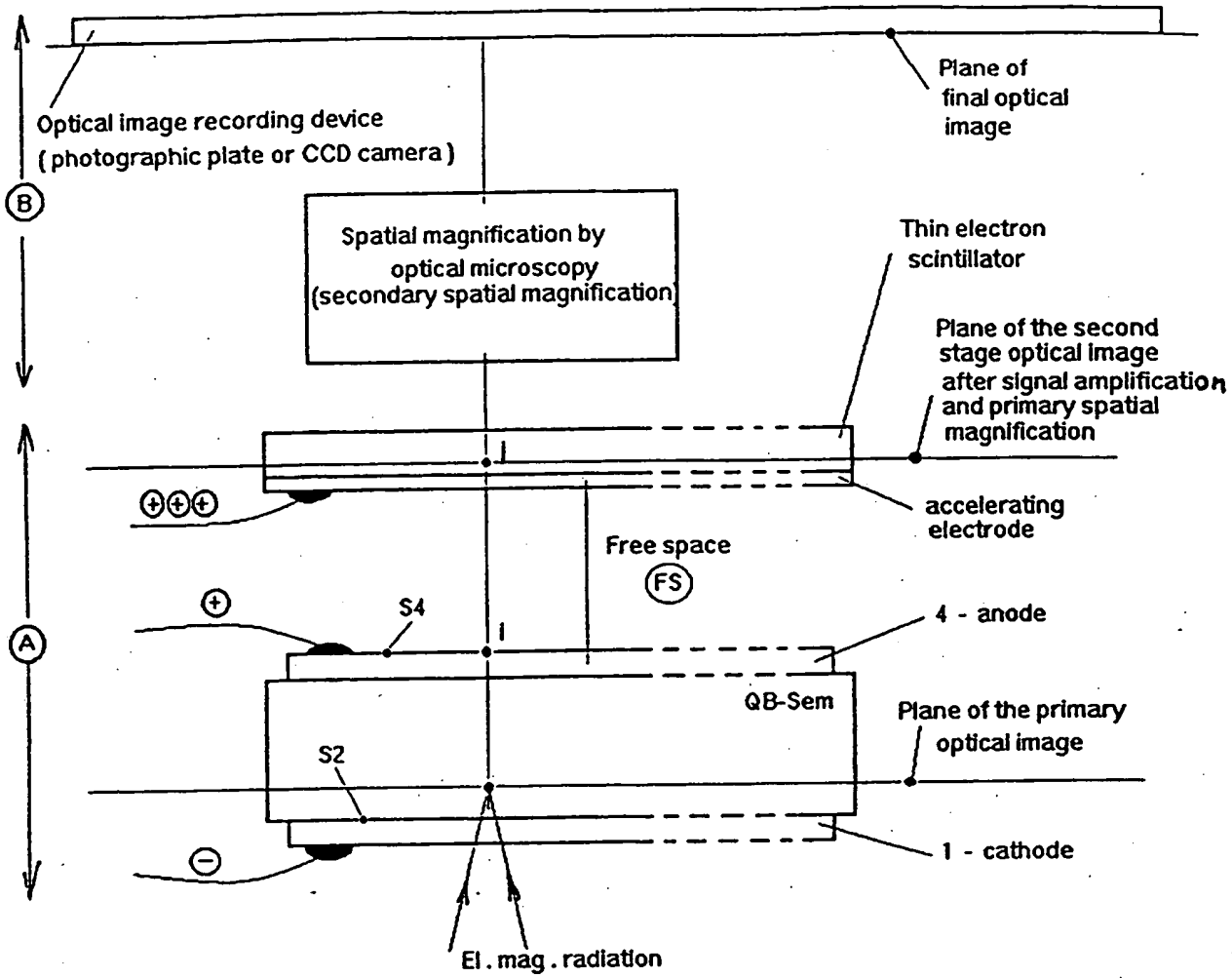
Optical image recording device
(photographic plate or CCD camera)
Plane of
final optical
image
B
Spatial magnification by
optical microscopy
(secondary spatial magnification)
Thin electron
scintillator
Plane of the second
stage optical image
after signal amplification
and primary spatial
magnification
accelerating
electrode
Free space
FS
S4
4 - anode
A
QB-Sem
Plane of the primary
optical image
S2
1 - cathode
El . mag . radiation

FIGURE 22

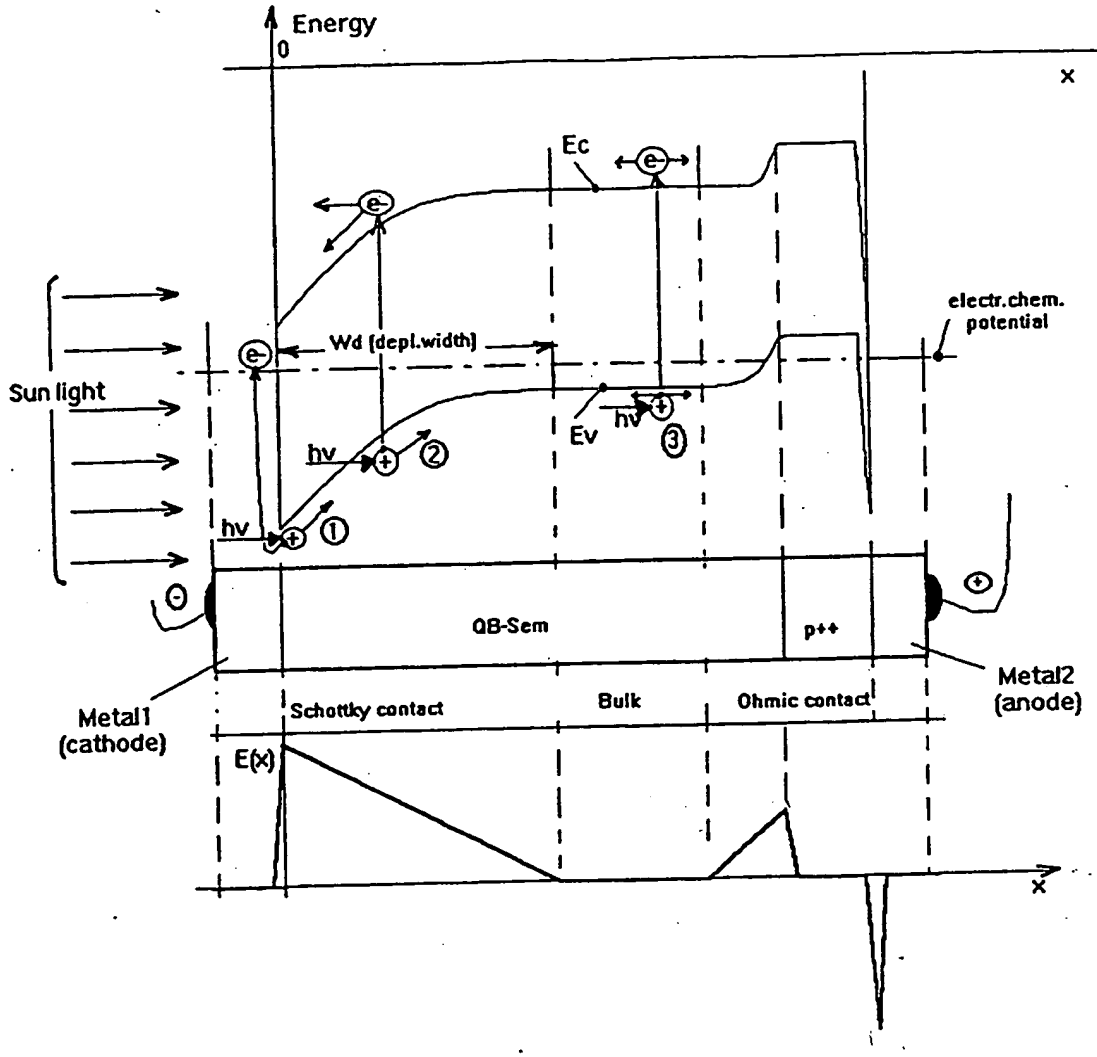
Energy
0
x
Ec
e-
Wd (depl.width)
electr.chem.
potential
Sun light
hv
Ev
hv
hv
1
2
3
QB-Sem
p++
Metal1
(cathode)
Metal2
(anode)
Schottky contact
Bulk
Ohmic contact
E(x)
x

FIGURE 23

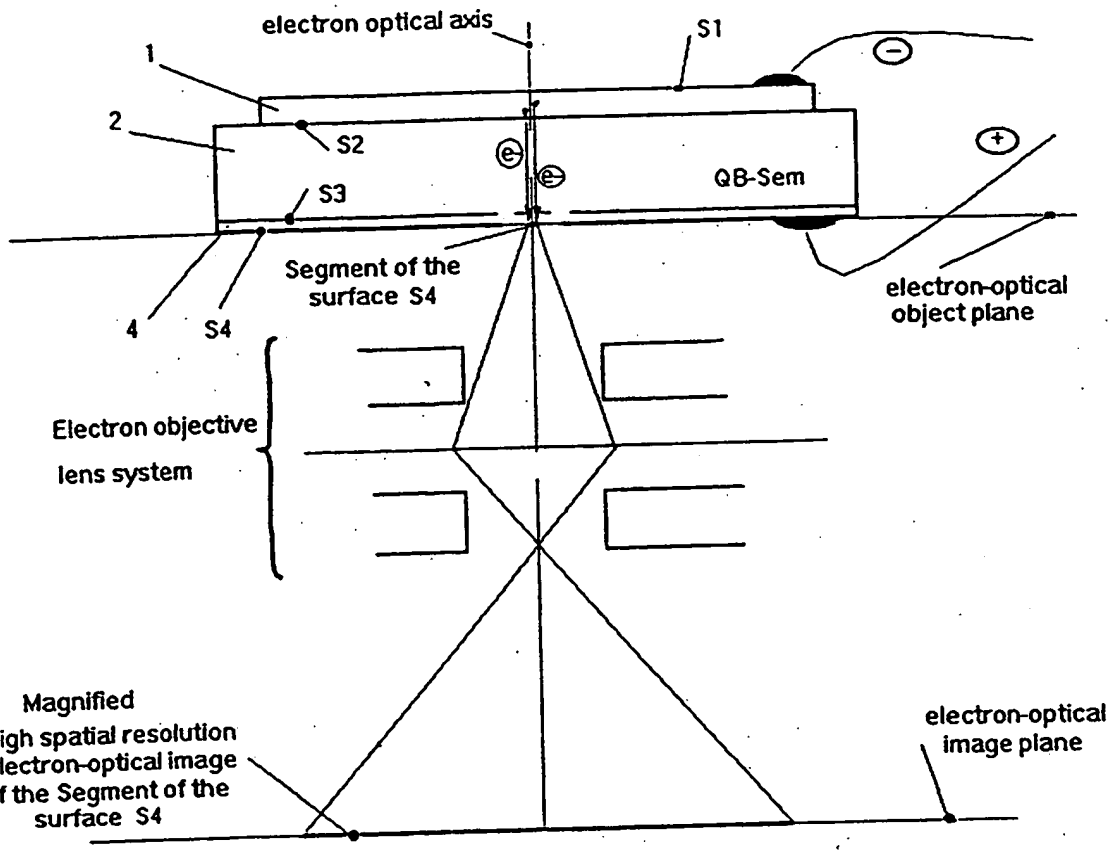
electron optical axis
S1
1
2
S2
S3
QB-Sem
Segment of the surface S4
4
S4
electron-optical object plane
Electron objective lens system
Magnified High spatial resolution electron-optical image of the Segment of the surface S4
electron-optical image plane

FIGURE 24